Ku/K-Band LTCC SMD Circulator for Space Applications

15-18 October 2024
ESA/ESTEC, Noordwijk, The Netherlands

S. Jemmeli [(1)], H. Turki [(1)], I. Marah [(1)], J.L. Roux [(2)], C. Karnfelt [(3)], R. Lebourgeois [(4)]
[(1)] *Exens-Solutions, France*
[(2)] *CNES: French Space Agency, France*
[(3)] *IMT Atlantique, France*
[(4)] *Thales Research and Technology, France*

Email: Sarra.jemmeli@exens-solutions.com

INTRODUCTION

In light of the increasing need to meet the RF systems requirements, circulators, as key components, have been the subject of research for several years. Conventional circulators are commonly based on Y-junction shape designed in stripline or microstrip technology. Stripline circulators are simple to integrate and induce low losses. This circulator topology can be connectorized through coaxial connectors, realized in a Drop-in technology or built in a Surface Mount Device (SMD). Despite their higher cost, coaxial circulators have higher EMC shielding and power handling capabilities than others. Furthermore, Drop-in devices handle less power and have no EMC shielding. Finally, SMD circulators have lower power handling capability than coaxial circulators but have better EMC shielding than Drop-in. Facing the growing need of miniaturization, integration, and cost reduction, the LTCC (Low Temperature Co-fired Ceramics) technology is a promising candidate to meet these challenges. LTCC technology is a technique for housing integrated circuits through a multilayer structure. It consists of stacking tapes, which prevents air gaps in the junction, and reduce multipaction risks for high power space applications. In the past years, many published studies focused on the design of LTCC circulators [1]-[2]. Nevertheless, most of them were theoretical and only a few focused on industrial purposes [3]. Hence, Exens-Solutions, in collaboration with CNES, Thales TRT and IMT Atlantique, have proposed LTCC technology to develop a K-band circulator to protect active antennas. The circulator is designed by Exens-Solutions based on specifications agreed with CNES. IMT Atlantique is in charge of the circulator manufacturing process. The ferrite and dielectric materials tapes are developed by Thales TRT.
Thus, the present paper is divided into four sections. The first section presents the LTCC circulator specifications and details the materials properties. A dry run to establish the design rules is described in the second Section. The design steps and simulations of the LTCC circulator are discussed in the third Section. The manufacturing steps and measurement results are reported in the last Section.

LTCC CIRCULATOR SPECIFICATIONS

Preliminary proposed topology

The stripline topology is adopted for the design of LTCC circulators housed in their packages. This topology has the advantage of miniaturizing the circulator and avoiding any damage of the metal paths. As shown in Fig.1, signal and ground vias are added to the LTCC structure to ensure its interconnection with an SMD surface.

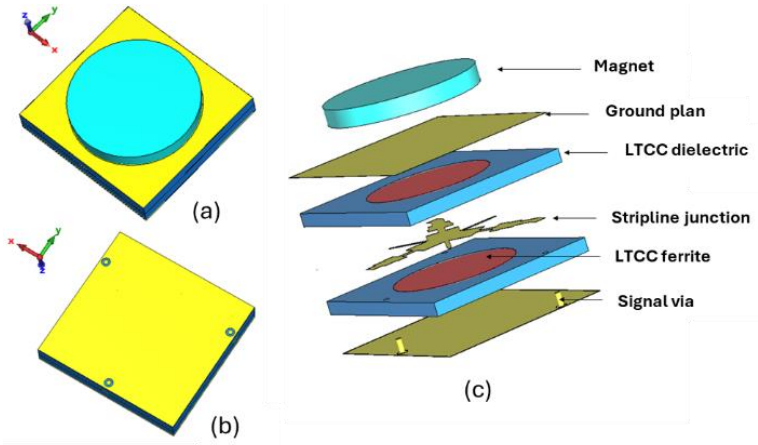


Fig. 1. Preliminary illustration of the stripline LTCC circulator, (a) top view, (b) bottom view and (c) detailed view.

RF characteristics

The selection of ferrite and dielectric characteristics is made to achieve the requested performances detailed in Table 1. To ensure an optimum functioning of the LTCC circulator in the desired frequency band (16GHz-22GHz), a weak-field polarization is required. The choice of the ferrite saturation magnetization is based on the Equation (1):

$$\frac{f}{3\gamma} < M_s < \frac{3f}{4\gamma}$$
$$2261 < M_s < 5089 \quad (1)$$

Table 1. LTCC circulator specifications

		Initial target		Long term target	
Parameters	Unit	Min	Max	Min	Max
Frequencies	GHz	17.3	20.2	16	22
Insertion loss	dB	-	0.7	-	0.5
Losses variation	dBpp	-	0.1	-	0.1
Isolation	dB	15	-	20	-
Return loss	dB	15	-	20	-
Power handling	W	-	1	-	10
Dimensions	mm3		5x5x4		5x5x3

For this first development, a power handling of 1W is required, hence the choice of a non-doped ferrite that will minimize insertion losses. Given these characteristics, an NZC38 (Nickel-Zinc-Copper) ferrite is proposed by THALES TRT with a high saturation magnetization (*Ms*) and a permittivity of 14. As for the dielectric, two materials have been suggested: the first with permittivity of 14 and 21 for the second. The material selection will be done after electromagnetic simulations.

Ferrite material validation: test vehicle

A test vehicle is suggested to validate the operation of the ferrite proposed by THALES TRT in the targeted frequency band.

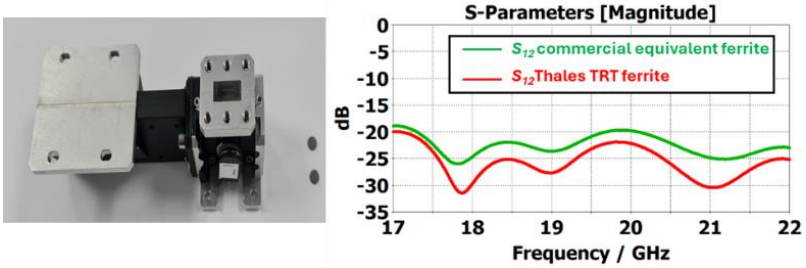


Fig. 2. Test vehicle isolation comparison results between commercial equivalent ferrite and Thales TRT ferrite.

Thanks to its low manufacturing dispersion effects due to limited mechanical and assembly tolerances, a rectangular waveguide isolator (RWG) with a WR51 flange is chosen. The RWG offers greater flexibility in gluing and ungluing the ferrite, which facilitates comparison between the ferrite proposed by THALES TRT (NZC38) and a conventional ferrite from Exxelia [5]. The latter was chosen for its characteristics, which are sufficiently close to those of THALES TRT to allow a better comparison. These two ferrites were tested on the same RWG after in-house machining. The measured isolations, with each ferrite, are shown in the Fig.2. The measurements comparison shows a good agreement between these two configurations. A slight non-conformity is observed due to the difference in *Ms* and ε_r of the two materials. The performance of the RGW remains satisfying and validates the correct operation of the TRT ferrite in the targeted frequency band.

DRY RUN & DESIGN RULES

This preliminary study was carried out by IMT Atlantique to acquire a better understanding of the manufacturing phases and constraints of LTCC circulators in stripline technology. The developed prototypes are not fully functional and are based on LTCC tapes already available at IMT Atlantique (A6M-E). The coplanar structure consists of a stack of 15 layers of A6M-E (Fig.3), the last 5 layers are fugitive tapes with inserts to house the magnets.

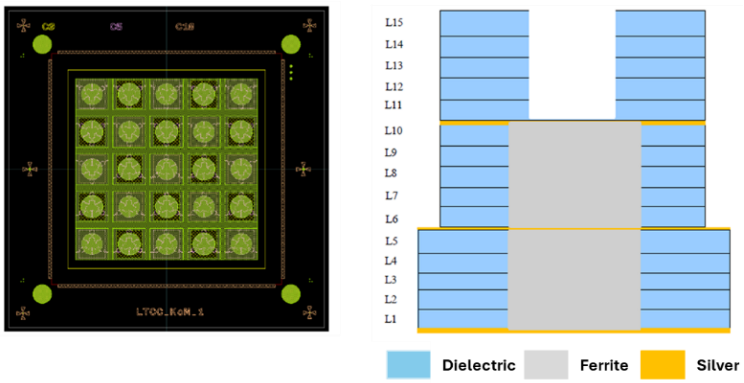


Fig. 3. Dry Run: Preliminary realization of a stripline LTCC circulator based on A6M-E layers.

This prototype highlighted several issues to be considered during the final phase of the circulator's development. The non-planarity of the surface of the ferrite layers led to a metallization problem during the screen-printing and drying phases, as shown in Fig.4. However, this problem is unlikely to occur with the tapes made by Thales TRT. For a more reliable design, the L6-L10 layers will be replaced with dielectrics. The minimum number of layers is set at 5 with a thickness of 102,5µm after the circuit firing process. The metallized layers are connected through vias with a minimum diameter $Ø_{via}$=80µm. To ease their filling with conductor material, the vias are surrounded with catch pad ($Ø_{catch\_pad}$= $Ø_{via}$+100µm) on each layer.

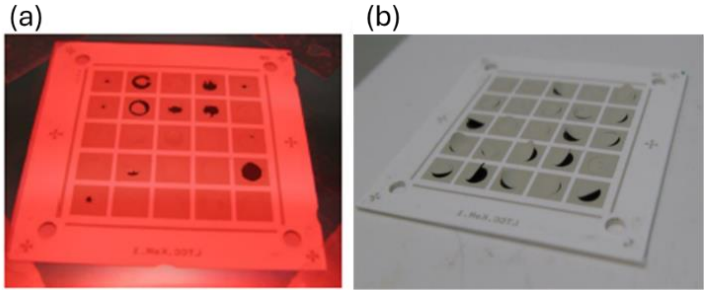


Fig. 4. (a) Metallization default after screen printing process, (b) Metallization removal problem and ferrite detachment during the drying phase.

All these manufacturing constraints allowed to define design rules to be applied for the final phase of the LTCC circulator manufacturing.

DESIGN AND SIMULATION OF LTCC CIRCULATOR

Circulators in LTCC technology are a good alternative for more robust and automated design. As a result, it is crucial to strengthen the simulation reliability. Unlike for other topologies, LTCC circulators are not tunable once prototyped. Therefore, their optimization process should be controlled, and all simulation constraints must be considered.

Stripline junction

The first simulations aimed to define the stripline topology. The number of ferrite and dielectric layers and the junction dimensions are optimized to obtain better performances in the operating frequency band. The chosen structure consists of a stack of 2 dielectric ($\varepsilon_r=14$) bottom layers with 3 upper ones separated by a stripline junction. Two ferrite NZC38 layers are embedded into the bottom dielectric and two ground planes are placed at the upper and lower sides of the circulator. The whole structure is shielded by adding ground vias, which reduce-insertion losses (Fig.5). The device is fed through waveguide ports with an input impedance of 50Ω.

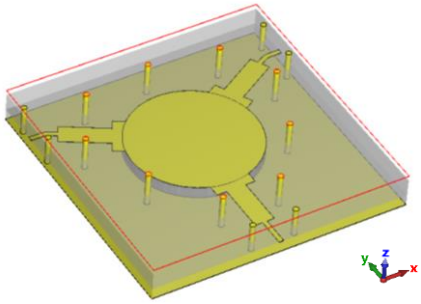


Fig.5. Preliminary design of the LTCC circulator.

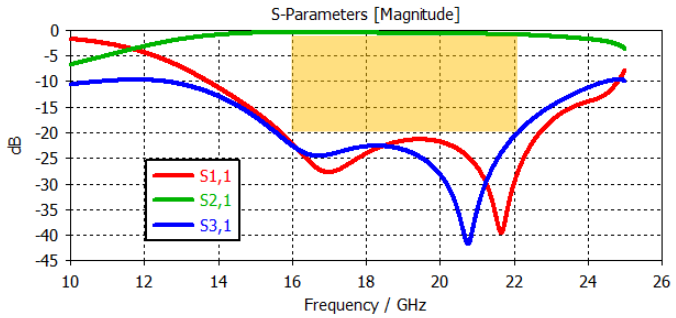


Fig. 6. Preliminary LTCC design simulation results.

The simulation results, in terms of return loss, isolation and insertion losses are illustrated in Fig.6. From these curves, it is obvious that the results are compliant with the specifications. The return loss on the 3 ports is less than -20dB over the entire frequency band. The isolation also meets the specifications (<-20dB). Regarding the insertion loss, they are lower than 0.5dB. However, they remain approximative and should be confirmed after measurements.

LTCC circulator fed through CPW-to-stripline vertical transition

Once the preliminary approach is validated, the challenge is to develop an LTCC circulator optimized for reliable production. The idea was to consider a coplanar waveguide (CPW) to stripline vertical transition to ease the device integration into SMD technology [4]. The parameters of the CPW-stripline transition are set to respect the design rules and to obtain an impedance of 50Ω. Consequently, an intermediate ground plane is designed on the third dielectric tape layer. Ground vias are also added to the structure to obtain a better shielding. The designed LTCC circulator with the CPW-stripline transition is shown in Fig. 7.

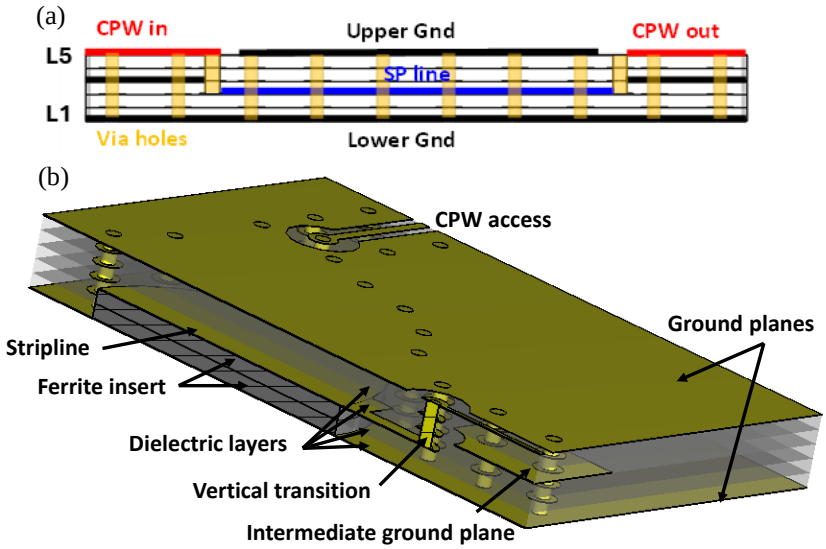


Fig. 7. Design of the LTCC circulator fed with a CPW-Stripline transition. (a) layer view, (b) Section view.

The S parameters of the circulator are shown in Fig.8. These results show good impedance matching in the full operating frequency band with return loss and isolation below -20 dB up to 21.5 GHz. Regarding insertion losses, they are approximatively lower than 0.5dB.

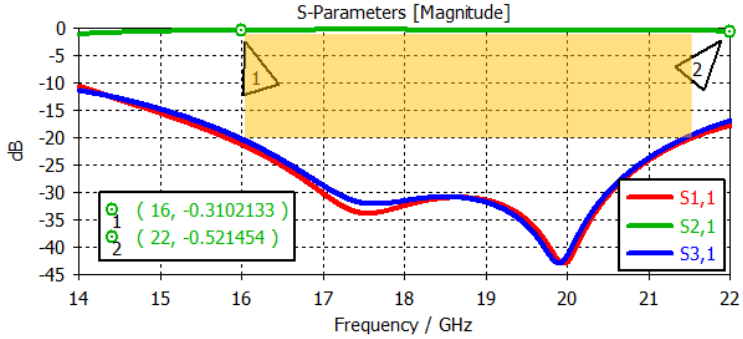


Fig. 8. LTCC circulator simulated S parameters.

Once the simulation results are compliant with specification, the manufacturing process can start.

MANUFACTURING OF THE CIRCULATOR

The device layers configuration is transmitted to IMT Atlantique to implement production. The circulators are built with five layers, which include ferrite inserts in two of them. On the same wafer, the test transmission lines (Fig.9 (a)) are integrated to measure the CPW-stripline typical transmission loss. The first realization step consists in cutting the via holes and cavities using a Nd:YAG 1064nm laser (Fig.9 (b)-(c)). The vias are then filled with conductive material (Fig.9 (d)). Conductor patterns are subsequently screen-printed using gold paste, which is more suitable for ferrite material (Fig.9 (e)). Screen printing is followed by stacking the different layers, which allows them to be assembled and better aligned. Before that, the ferrite inserts are placed in the dedicated cavity. The structure is then laminated to avoid any air gaps between its different layers. The top gold on the ferrites is screen printed before the circuit is fired at a temperature of 920°C (Fig.9 (f)). Finally, measurements are done on a probe station with thermal chuck, using 150 µm pitch GSG probes and a 67 GHz VNA. These CPW measurements aim to validate the LTCC circulator topology. Although, for commercial purpose, SMD pads will be added to the device to ensure interconnexion with the end user RF system.

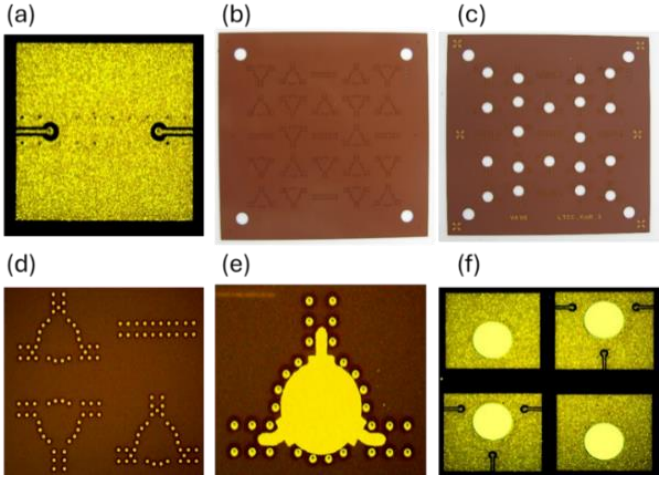
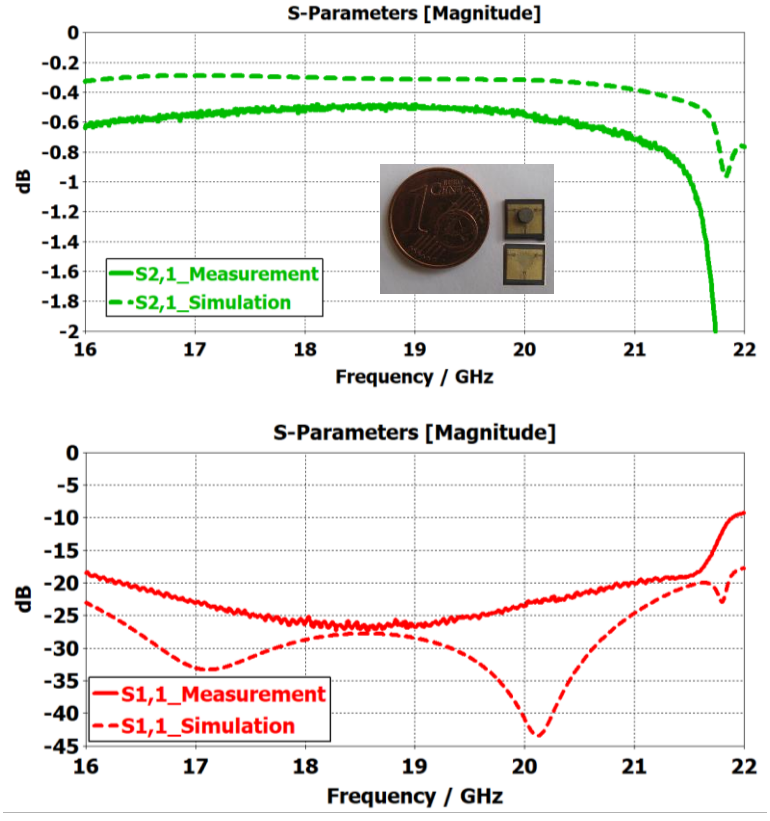


Fig. 9. Fabrication process, (a) test transmission line with ground plan vias, (b) via holes cutting, (c) ferrite cavity inserts creating, (d) via holes filling, (e) conductor patterns screen-printing, (f) top gold screen printed.



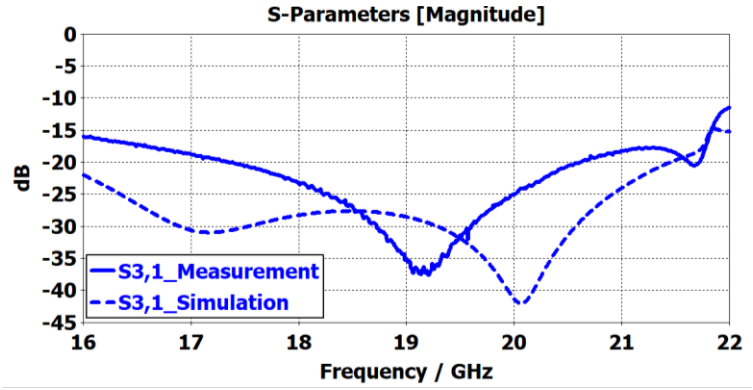


Fig. 10: Measured S parameters Vs simulated S parameters.

Table 1. Comparison of the requested and obtained LTCC circulator performances.

	Specification		**Measured results**	
	Typical	**Max**	**Typical**	**Max**
Frequencies (GHz)	[17-22]	[17.3-20.2]	[16-21]	[17-20.5]
Insertion Loss (dB)	0.5	0.7	0.6	0.57
Return Loss (dB)	20	15	19	22
Isolation (dB)	20	15	16	19
Dimensions (mm^3)	5x5x4	5x5x3	5.48x4.6x2.5	

CONCLUSION

A Ku/K-band LTCC circulator is presented in the current paper. The design process is also detailed, and the simulation results discussed. The device is built with 5 layers of dielectric and 2 ferrite disk inserts. The circulator is fed through CPW-stripline vertical transition for future integration purposes. The fabrication steps are shown, and the measurement results are in alignment with the simulated performances, meeting the initial target specifications.

ACKNOWLEDGEMENT

The present work has been carried out as a part of a Research and Technique study in collaboration with CNES (Centre National des Etudes Spatiales). Exens-Solutions (https://www.exens-solutions.com/index.html) would like to acknowledge its collaborators: Thales TRT for the materials development and IMT Atlantique for prototype manufacturing.

REFERENCES

[1] [1] R. van Dijk, G. van der Bent, M. Ashari and M. McKay, “Circulator Integrated in Low Temperature Co-Fired Ceramics Technology”, *9th European Microwave Integrated Circuits Conference*, December 2014, Rome, Italy.

[2] S. Yang, W. Shi, H. Bai and T. Zhang “Circulator integrated in LTCC with screen printed cofiring ferrite for space application”, *International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, December 2018, Chengdu, China.

[3] C. Weil, T. Hauck, J. Schur and J. Müller, “Broadband Ku- and Ka-Band Circulators in LTCC Using Sintered Bulk Ferrites”, *Proceedings of the 51st European Microwave Conference*, June 2022, London, UK.

[4] A. Bhutani, B. Goettel, T. Thelemann and T. Zwick, “CPW-to-SL transition in LTCC technology”, *Electronics Letters*, 27th April 2017 Vol. 53 No. 9 pp. 609–611.

[5] Exxelia. https://exxelia.com/uploads/PDF/a-series-v1.pdf

Wideband Design of Very High Power L-band Isolator for Galileo's Next Generation

15-18 October 2024
ESA/ESTEC, Noordwijk, The Netherlands

T-T. Pham, I. Marah, J-C. Plumecoq, R. Tyan

Exens-Solutions
3, Avenue du Pacifique
91940 Les Ulis - France
Email : tien-thong.pham@exens-solutions.com

ABSTRACT

This paper presents the design and simulation of a wideband isolator tailored for space applications within the L-Band frequency range, intended for integration into the next Galileo program. The isolator, measuring 81.3mm x 76.8mm x 24.6mm, integrates a Y-junction circulator loaded with a high-power load, capable of handling 280W continuous wave power. Through extensive simulation, the isolator demonstrates promising performance metrics, including an insertion loss, return loss, and isolation of 0.25dB, 18.7dB, and 19.2dB, respectively, over the frequency band of 1140MHz to 1605MHz. The implementation of high-power connectors (TNC VHP-C) effectively mitigates multipactor effects and ensures robust thermal behavior, providing a safety margin of 60°C. This work underscores the feasibility of the proposed isolator design for the upcoming Galileo program.

INTRODUCTION

Advanced technologies could significantly enhance future Positioning, Navigation and Timing (PNT) systems capabilities in terms of cost and time to market while providing adequate performance for the application. In addition, new PNT constellation based on small satellites in LEO/MEO/IGSO orbits are under assessment. The implementation of PNT payloads on small platforms or as hosted payload will affect the technological solutions since, they will require reduced size and mass equipment. New concepts and production approaches need to be optimized for the near future, carefully considering cost and time to market.

This study is focused on the design of a wideband high power isolator for navigation payload output section to market PNT systems in MEO orbit, specially for the Galileo program [1]. Within the activity, the potential re-use of technology solutions and concepts are also investigated.

TECHNICAL DESCRIPTION

The high power isolator proposed in this study is shown in Fig. 1, and is composed of a Y-junction circulator [2],[3] with an integrated high power termination. The circulator is a passive non-reciprocal three-port device with TNC connectors. It is based on stripline technology and is composed of magnetized ferrite materials. The anisotropic properties of these materials ensure the non-reciprocal character of the wave propagation. The circulator's junction has silver plated aluminum ground planes and ferrite disks located on each side of the stripline.

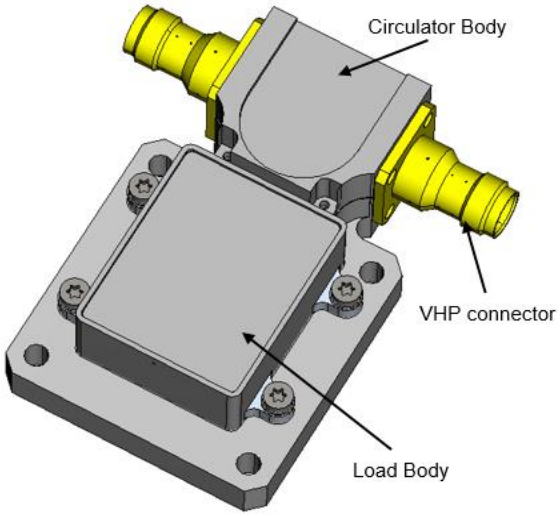


Fig. 1. 3D view of the proposed TNC High Power Isolator

Permanent magnets and polar disks are added to bias the circulator's junction. To ensure thermal stability, magnetic compensators are also used. Finally, a steel yoke is placed on the circulator's body to shield the magnetic circuit. The circulator is polarized in a region beyond the gyromagnetic resonance, resulting in no performance limitation coming from non-linear effects. The ferrite material shows a good stability in temperature range along with low insertion losses. Very High Power (VHP) TNC connectors [4] are selected for high power handling. Moreover, the isolator is filled with potting glue to suppress any potential multipactor risk.

ELECTRICAL DESIGN

Simulation model

This isolator has been simulated with CST software and a simplified model with a third port loaded is shown in Fig. 2:

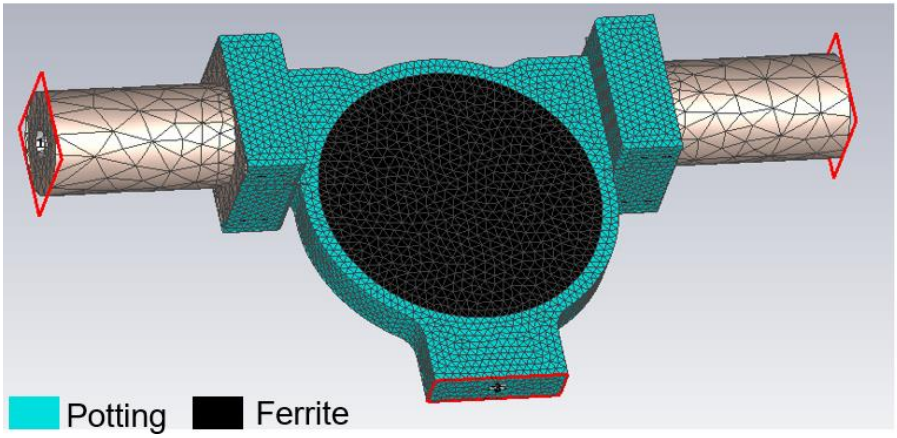


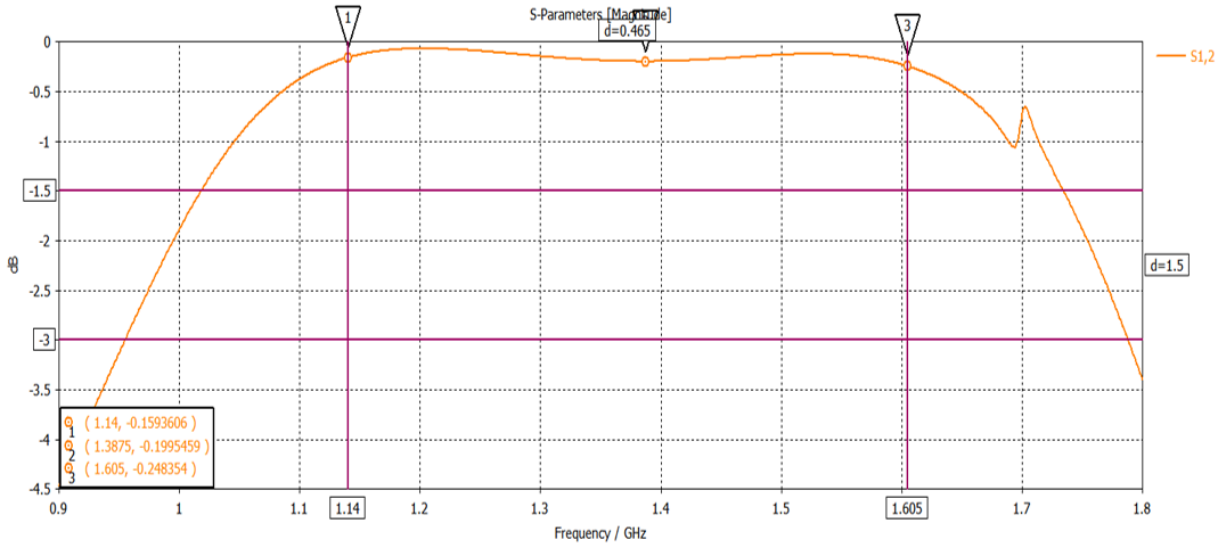
Fig. 2. Simulation model of the L Band High Power Isolator

The following main parameters have been used for this simulation:

Potting: Glue - Space-Grade and qualified
Ferrite: Y-family
Isolator body: 32mm x 27mm.

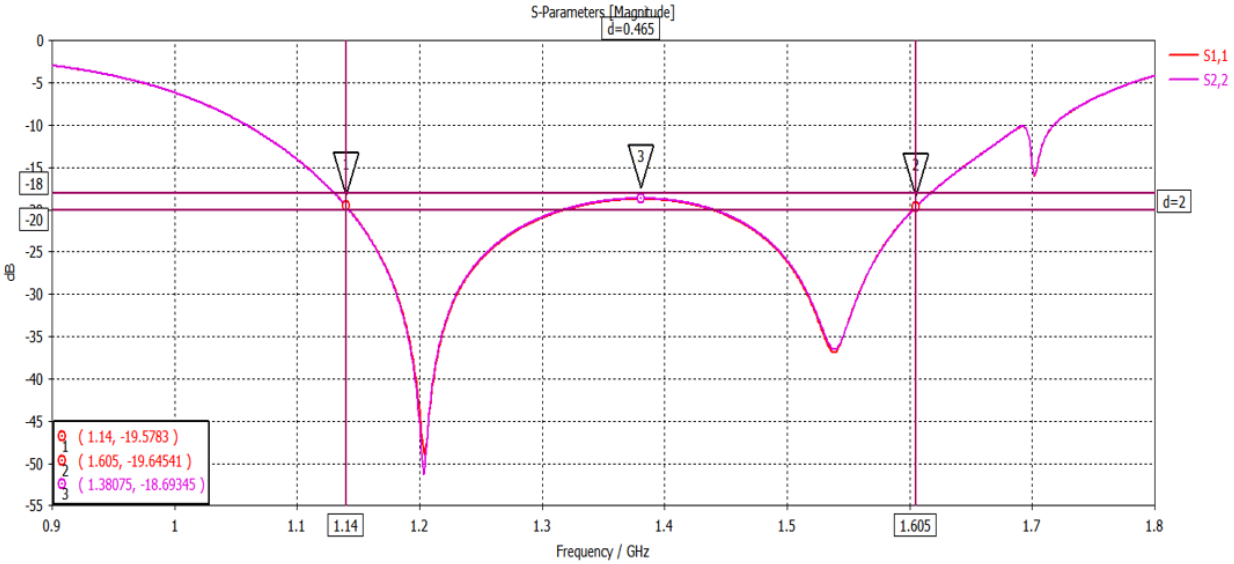
Simulation results

The S-parameters simulation results of are presented in Fig. 3, Fig. 4 and Fig. 5.



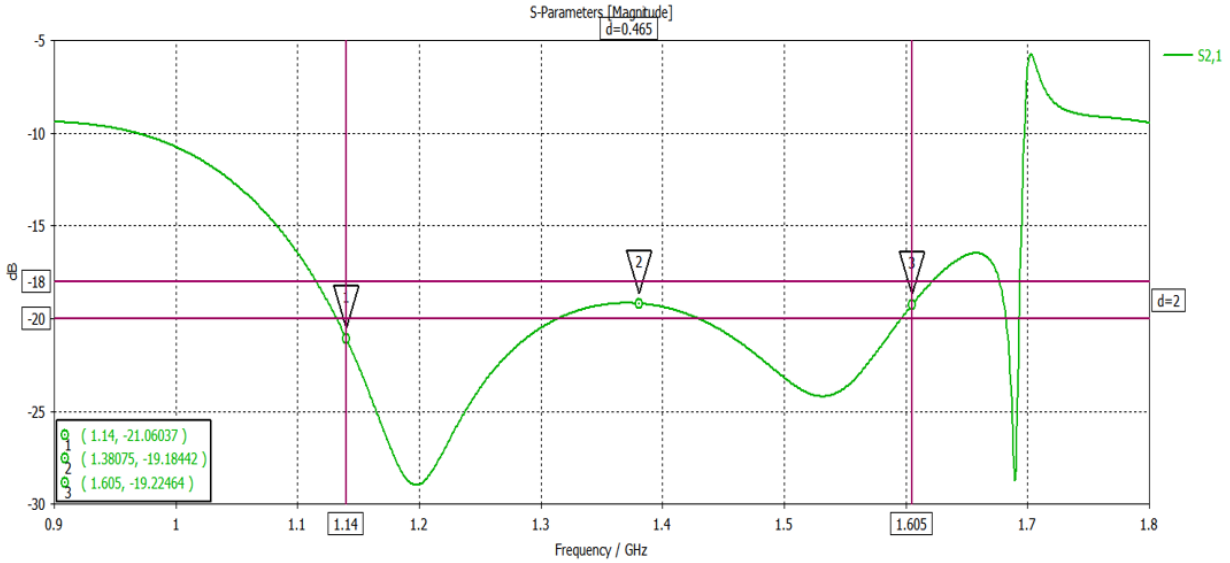
Parameters	Specifications	Worst Case
Insertion Loss	0.25 dB	0.25 dB

Fig. 3. Insertion loss of the proposed isolator



Parameters	Specifications	Worst Case
Return Loss	21 dB	18.7 dB

Fig. 4. Return loss of the proposed isolator



Parameters	Specifications	Worst Case
Isolation	21 dB	19.2 dB

Fig. 5. Isolation of the proposed isolator

A simulation of this isolator with existing measurement data of resistive chips has also been performed. The simulation model is shown in Fig. 6, and a comparison with previously simulated S-parameters without measured load is also presented in Fig. 7.

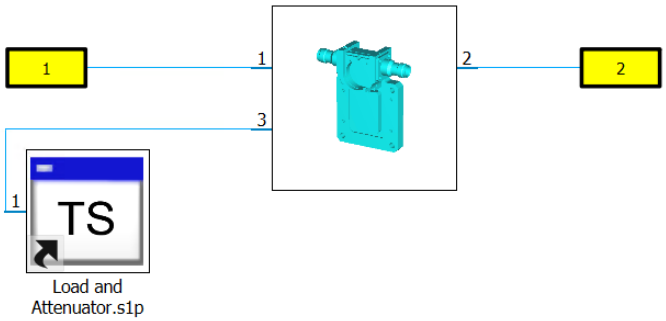


Fig. 6. Simulation model of the High Power Isolator with the load and the attenuator

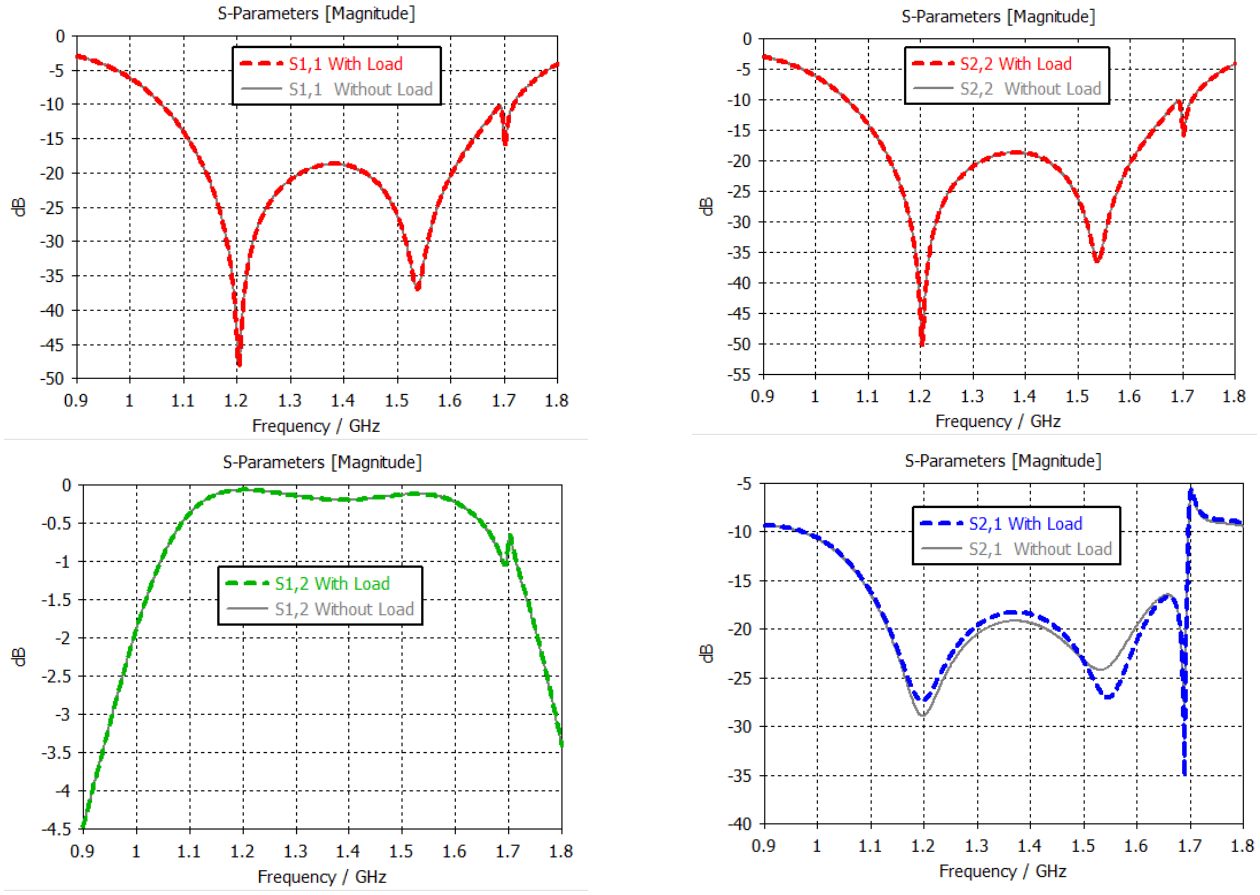


Fig. 7. Comparison between the S-Parameters of the simulation model with and without load

There is a good correlation overall, but also a slight difference for isolation. However, these performances could be improved by tuning after manufacturing.

HIGH POWER ANALYSIS

To evaluate power handling capability of this high power isolator, a thermal simulation and a multipactor analysis are performed and described in the following sections.

Thermal simulation

The contact coefficient between the isolator contact area and the conductive interface has been set to a standard value in $W/m^2/°K$. The base plate temperature considered in this analysis is 60°C.

In order to perform thermal simulations on the proposed isolator, an electromagnetic simulation has been performed with CST software. This simulation allows to extract the distribution map of the volume density of the electromagnetic losses in the isolator. These losses are dielectric, metallic and ferromagnetic. Once the volume loss distribution is established, then it is injected in the thermal solver of CST. The losses considered in this analysis correspond to the worst-case operation of the circulator losses, and are represented by 0.3 dB insertion losses of the circulator at 60°C. A thermal analysis has been performed with Thermal Steady State CST solver, version 2021 SP5. The input power of the isolator is 280 W in continuous wave. To study the worst case of the isolator, its output port is short-circuited.

The thermal simulation is performed with a mesh of 175955 points as shown in Fig. 8. The temperature map of the isolator with 280 W CW input power and short circuited output is presented in Fig. 9. with maximum temperatures in Table 1.

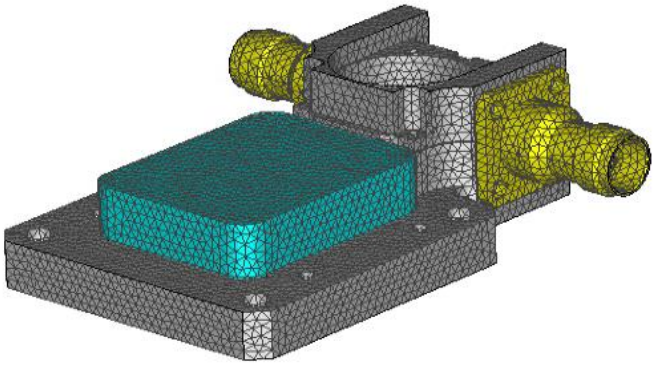


Fig. 8. Mesh view of the simulated isolator

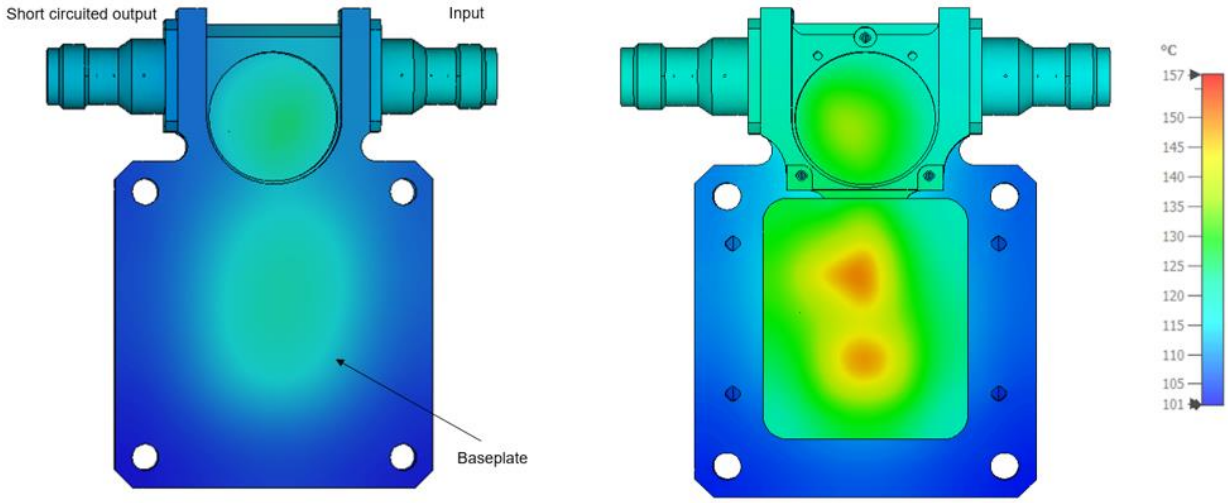


Fig. 9. Temperature map of the simulated isolator

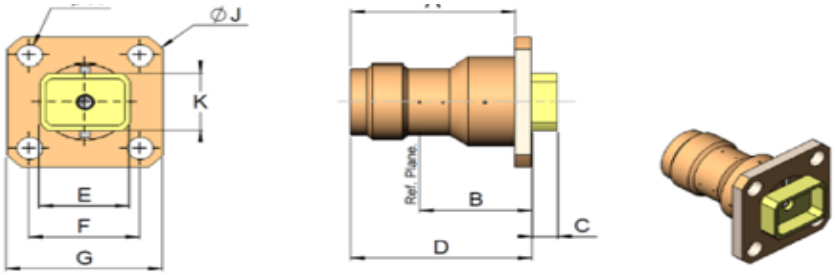
Materials	Maximum calculated temperature (^{0}C)
Aluminium	125
Ferrite	130
Potting	130
Resistive chip	160
Soldering	150
Coating	128

Table 1. Maximum simulated temperatures

According to simulation results and qualification temperatures, the proposed isolator is compliant with the required power in a short-circuited output operation with a minimum margin of 60 °C.

Multipactor Analysis

The proposed isolator is filled with potting glue so that it considered a multipactor free design. As a consequence, the multipactor threshold will be that of the VHP TNC connector, which has a multipactor free level of more than 2000 W (Fig. 10) obtained by test.



ELECTRICAL CHARACTERISTICS	MAXIMUM VALUES	UNITS	REMARK
Frequency Band			-
L Band	1 to 2	GHz	
C Band	4 to 8	GHz	
Power Handling:			
L Band	400	W CW	
C Band	300	W CW	
Multipactor threshold			
L Band	≥2000	Wpp	Max. tested values, pulse width 20µs; PRF 1000Hz
C Band	≥2000	Wpp	
Corona threshold			
L Band	≥120	W	
C Band	≥100	W	
Maximum Voltage Standing Wave Ratio (VSWR)			
L Band	≤ 1.1+0.02 x F	-	F in GHz
C Band	≤ 1.1+0.02 x F	-	
Maximum Insertion Loss			
L Band	≤ 0.12√F	dB	F in GHz
C Band	≤ 0.12√F	dB	
RF Leakage	≥ -115 + F	dBi	F in GHz
Operating Temperature Range	-65 to +165	°C	See figure 1(b)
Contact Resistance			
Centre contact	≤ 4	mΩ	At +25°C, 20mV, 10mA
Outer contact	≤ 4	mΩ	At +25°C, 20mV, 10mA
Mini centre contact retention force (axial)	27.2	N	
Mini centre contact retention torque	2.8	N.cm	
Passive Inter Modulation (PIM): Order7			
L Band	-140	dBm	With two carriers of 50W

Fig. 10. Used connector power handling [4]

CONCLUSIONS AND PERSPECTIVES

This study demonstrated the feasibility of a wideband high power isolator with a positive behavior regarding power handling and multipactor capabilities thanks to:

- The use of very high power connectors (VHP TNC) with slightly more losses than “standard” one.
- The addition of potting glue in the junction to become multipactor free.

In conclusion, electrical performances of insertion loss, return loss and isolation of 0.25dB, 18.7dB, and 19.2dB, respectively, over the frequency band from 1140MHz to 1605MHz, were obtained in this work. The isolator performances can be improved by tuning methods during the prototyping. Due to the size of the VHP TNC connectors, the final dimension of this isolator is 81.3mm x 76.8mm x 24.6mm. The proposed isolator also demonstrated a good thermal behavior with a safety margin of 60^0C.

REFERENCES

[1] Galileo Second Generation
http://www.esa.int/Applications/Navigation/Galileo next gen satellites on the horizon

[2] D. M. Pozar, *Microwave Engineering, 2nd. Ed.*, Wiley, 1996.

[3] H. Turki, L. Huitema, T. Monediere, B. Lenoir and C. Breuil, “Complete Methodology of Low-loss Ultra-wideband Junction Circulator”, *2018 IEEE/MTT-S International Microwave Symposium – IMS*, Philadelphia, PA, 2018, pp. 746-749.

[4] Detail Specification, “RF Coaxial Connectors TNC Very High Power, 50 Ohms (Male & Female contact) DC – 8GHz”, 1st. *Ed.*, ESCC3402/TNCVHP-C, RADIALL, July 2015.

CRYOGENIC EVALUATION OF A COTS LATCHING RELAY

Conor Robinson [(1)], Erik Ryman [(1)], Sander Blommaert [(1)]

[(1)] European Space Agency
ESA ESTEC, Keplerlaan 1, 2201 AZ Noordwijk, The Netherlands
Email: conor.robinson@ext.esa.int
Email: erik.ryman@ext.esa.int
Email: sander.blommaert@ext.esa.int

INTRODUCTION

The Science department's Payload Validation section at ESA is responsible for the characterisation of payload technologies that are under development or may be utilised in planned European science missions. Within this context, relays that operate at cryogenic conditions are sometimes required within the lab for the purpose of switching between test conditions or signal paths.
Many of the payload technologies under evaluation are related to imaging, particularly at infrared wavelengths. These devices often operate at temperatures in the region of 60 K and are exceptionally sensitive to changes in temperature or comparatively warm objects in their field of view.
These constraints can often exclude standard non-latching relays as viable options due to the power dissipation of their coils. As such, a need for latching relays that would operate under high vacuum and in cryogenic conditions was recently identified to facilitate tests on a current project.
A sequence of tests has been carried out in the Payload Validation Laboratory on a custom test board containing nine Omron COTS G6KU-2F-Y DC3 latching relays, and has shown almost entirely nominal performance over more than 296,000 operations and 200 temperature cycles at temperatures as low as 47 K.
This paper will illustrate the context, test processes, results, and limitations of this evaluation.

BACKGROUND

In the 2015 paper 'High-gain cryogenic amplifier assembly employing a commercial CMOS operational amplifier' [1] , J. E. Proctor et al demonstrate a cryogenic amplifier for small current signals. In their paper, an Omron G6KU-2P-Y DC5 relay can be seen on the cryogenic test PCB that operates at temperatures below 10 K.
Following the disassembly and internal inspection of one of these relays in our lab, it was decided that the device would be a good initial candidate for use in our own cryogenic lab setups. As such, a test sequence was designed to evaluate their reliability at our own temperature of interest, namely 60K. In case the relays survived these main tests, an additional test was also designed for the evaluation of operability at the lowest temperature achievable in our cryostat.
The product series datasheet [2] states the operating temperature range of the relay as -40 to 70°C (equivalent to a range of 233 to 343 K), which is quite typical for COTS components. At this temperature range, the relay is mechanically rated to 50 million operations under no electrical load.

EXPERIMENTAL SETUP

As shown in Fig. 1, each relay has an individual drive input with both pairs of Normally Open (NO) and Normally Closed (NC) contacts connected to a common test point. These common NO and NC test points are shared between all nine relays. For the purpose of clarity, the position of the relay in which the moveable pole is touching the NC contact is called 'Reset', and the position where the pole is touching the NO contact is called 'Set'
The NO and NC contacts are connected to GND via different value resistors located on the test PCB, so that the resulting parallel resistance measurement indicates how many relays are in the Set and Reset states, and precisely which contacts are open or closed at any point. These resistor values were selected to ensure that any number of relays in Set and Reset states could be distinguished from one another, and that failures could be localised to a particular contact. Additionally, resistors with very low temperature coefficients were selected to ensure that the parallel resistance values were as consistent as possible over the temperature range of interest.

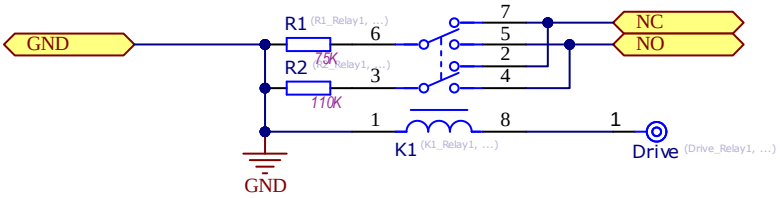


Fig. 1. Schematic layout of a relay test element in the 'Reset' position

The resulting PCB is shown in Fig. 2. This PCB also includes three active devices on the right-hand side, which were included to allow simultaneous cryogenic testing of op-amps for other lab purposes. The performance of these amplifiers is not within the scope of this paper, and it should be noted that these were not fitted when the relay tests described in this paper were being performed.

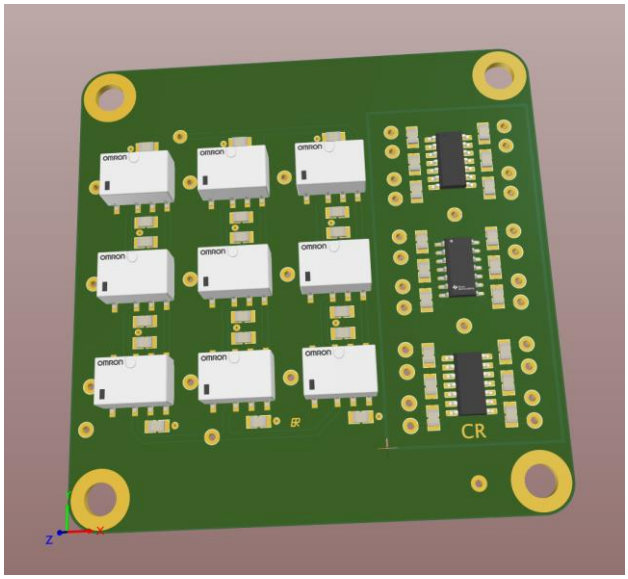


Fig. 2. 3D Rendering of the cryogenic relay test PCB

Before the PCB containing the relays under test was placed in the cryostat, the small plastic caps sealing the air mass inside the relay body were removed with a scalpel as shown in Fig. 3. This was done to reduce the risk of explosion within the cryostat from a trapped air volume within a vacuum environment. Once the caps are removed, it should be noted that the relays are much more vulnerable to contamination ingress.

Fig. 3. Relay with cap removed

The resulting PCB with de-capped relays was placed in SCI-FIV's 'BOXY' cryostat, shown in Fig. 4. This compact cryostat setup is used primarily for component testing and utilises a closed-loop helium cooling system with temperature regulation achieved using active heating elements.

The test equipment was controlled using a Python script which also recorded and saved the test data. The environmental conditions within BOXY were maintained using our custom laboratory test bench software environment 'Mistral'. Mistral is a Python-based server framework that facilitates communication with lab equipment and allows control of test benches via dynamic user interfaces and parameterised scripts.

Fig. 4. BOXY cryostat external view (left) and BOXY internal view showing installed test PCB (right)

The test PCB within the cryostat was connected to an Agilent E3631A Triple Output DC Power Supply, and an Agilent 34970A Data Acquisition/Switch Unit containing Multiplexer and Switch cards. A schematic diagram showing how these devices connect to one another is shown in Fig. 5. This setup allowed the control of DC power supply parameters, the switching of the DC output to different relays, and the continuous sampling of NO and NC contact resistances.

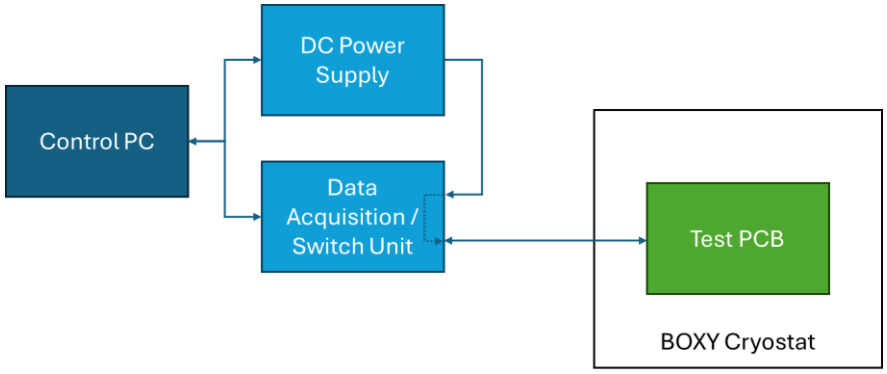


Fig. 5. Schematic layout of test equipment

The control script operated by maintaining a connection to the DC Power Supply and Data Acquisition/Switch Unit using standard GPIB protocols. The relays would then be toggled between their latch positions in sequence, as shown in Table 1. Both voltage and current limits were set on the DC power supply, as the relay coil resistances dropped significantly at cryogenic temperatures.

For each position change, values would be recorded for the coil voltage and current as well as for the measured resistance at the NO and NC contacts resulting from the combination of parallel resistances. The excitation current for resistance measurement was between 10 µA and 100 µA.

A failure counter was also maintained by the script, where a failure was defined as a resistance measurement that differed from the ideal by at least 2%. By recording errors against the step number, the individual relay at fault could also be identified and recorded.

Table 1 - Relay switching sequence and resulting ideal resistances

Step No.	Relay 0	Relay 1	Relay 2	Relay 3	Relay 4	Relay 5	Relay 6	Relay 7	Relay 8	NO Resistance	NC Resistance
1	Set	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	44.6 kΩ	5.7 kΩ
2	Set	Set	Reset	Reset	Reset	Reset	Reset	Reset	Reset	22.3 kΩ	6.6 kΩ
3	Set	Set	Set	Reset	Reset	Reset	Reset	Reset	Reset	14.87 kΩ	7.43 kΩ
…	…										
9	Set	Set	Set	Set	Set	Set	Set	Set	Reset	5.7 kΩ	44.6 kΩ
10	Set	Set	Set	Set	Set	Set	Set	Set	Set	5.1 kΩ	Open
11	Reset	Set	Set	Set	Set	Set	Set	Set	Set	5.7 kΩ	44.6 kΩ
12	Reset	Reset	Set	Set	Set	Set	Set	Set	Set	6.6 kΩ	22.3 kΩ
…	…										
18	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Open	5.1 kΩ

This process of opening and closing the relay contacts sequentially to add or remove parallel resistances leads to the distinctive ideal resistance graph with asymptotes shown in Fig. 6.
To clearly illustrate the proximity of the data points to the pass/fail criteria, graphs were also generated showing the difference between measured and ideal resistance values with the pass/fail criteria overlaid in green and red respectively, as shown in Fig. 7.

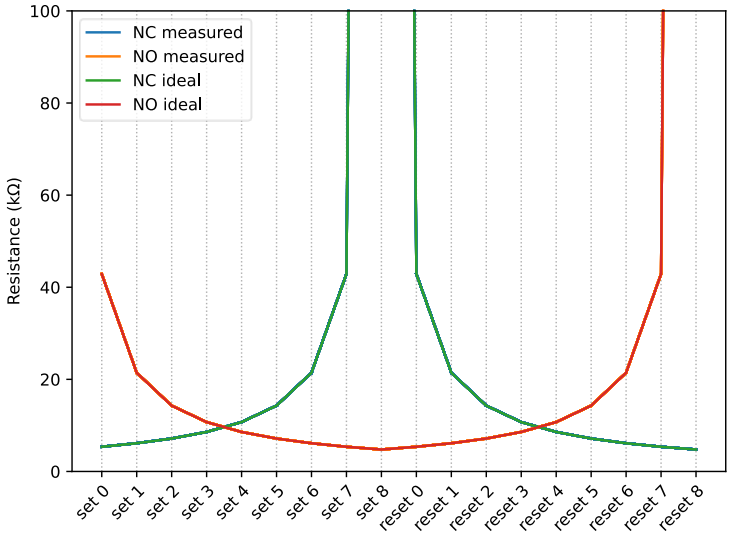


Fig. 6. Ideal and measured resistances for each test step.

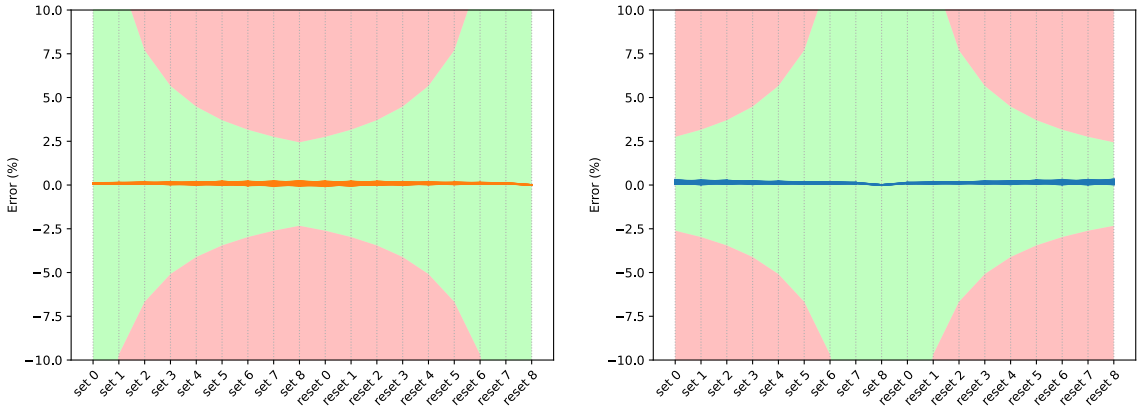


Fig. 7. Deviation from ideal resistance for the Normally Open (left) and Normally Closed (right) contacts.

TEST ONE – COLD START TEST

In the first test, the cold start test, the intention was to determine the behaviour of the relays when left at cryogenic temperatures and operated only occasionally. Due to the delicate nature of the contacts within the latching relays, it was theorised that any contamination within the device could freeze the contacts together and prevent the relay changing state.

Procedure

In the cold start test, the relays and test PCB were cooled to from room temperature to 60 K at a rate of 2 K/min and left to stabilise. The relays were then sequentially switched to 'Set' as described previously and left for two hours. Following the two-hour delay, the relays were sequentially switched to 'Reset' before another two-hour wait.

During this test, the relay coil voltage limit was 3 V, and the current limit was 40 mA. The switching pulse for the relay coils was 500 ms.

Results

The test was run for 118 hours (4.9 days), for a total of 60 switching cycles (120 operations per relay). Over this period, no failures were observed on any of the nine relays. Fig. 8 shows the log of relay failures over time for this test, and Fig. 9 shows the recorded values for deviation from the ideal resistance for each switching sequence.

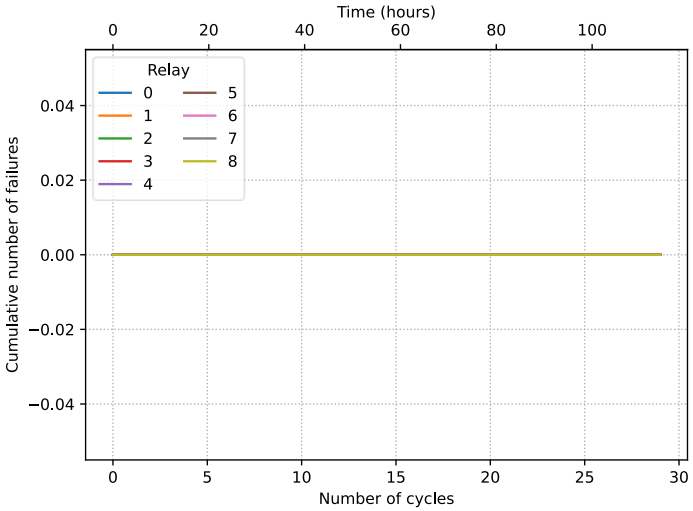


Fig. 8. Relay failures as a function of test time.

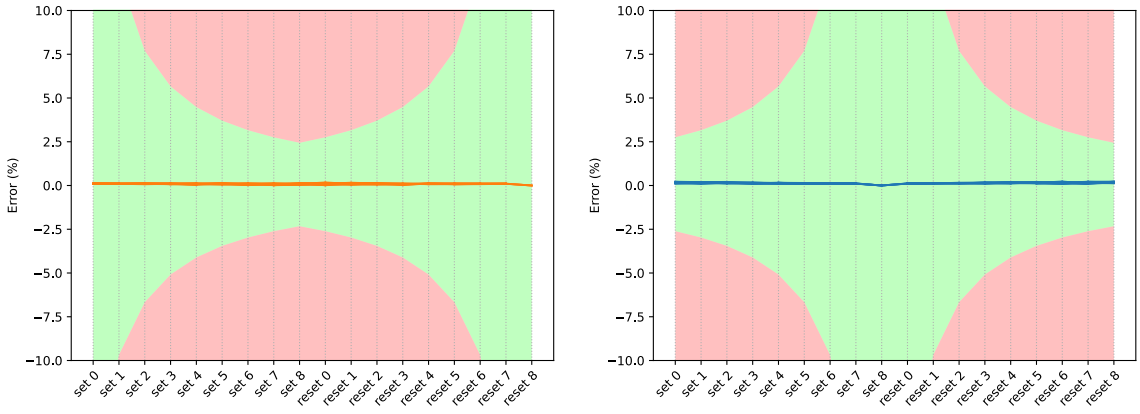


Fig. 9. Deviation from ideal resistance for the Normally Open (left) and Normally Closed (right) contacts.

TEST TWO – ENDURANCE TEST

In the second test, the endurance test, the intention was to investigate the longevity of the relays at the temperature of interest (60 K). It was theorised that the cryogenic temperatures may change how the relays age with continued use.

Procedure

The procedure for the endurance test was similar to that of the cold start test, insofar as the temperature was held at 60 K, the relay coil voltage limit was 3 V, and the current limit was 40 mA. The switching pulse for the relay coils was again set to 500 ms duration.

In this test, the delay between sequences was eliminated so that the relays were constantly running through the switching sequence. This gave a cycle duration of approximately 15 seconds.

Results

The test was run for 521 hours (21.7 days), for a total of 122,640 switching cycles (245,280 operations per relay). Over this period, no failures were observed on any of the nine relays. Fig. 10 shows the log of relay failures over time for this test, and Fig. 11 shows the recorded values for deviation from the ideal resistance for each switching sequence.

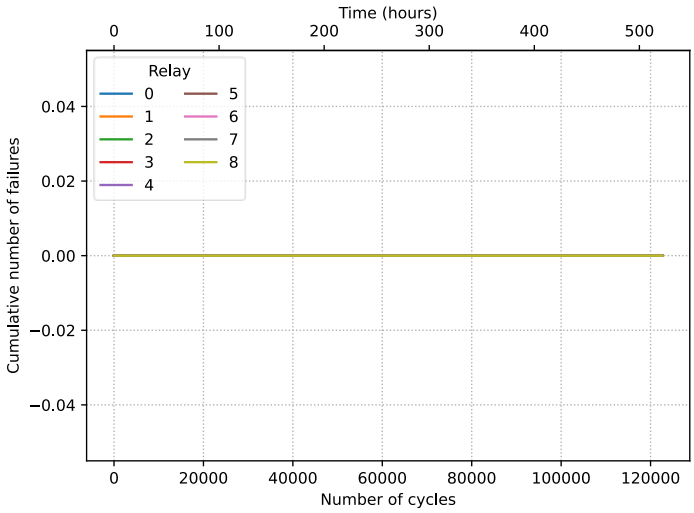


Fig. 10. Relay failures as a function of test time.

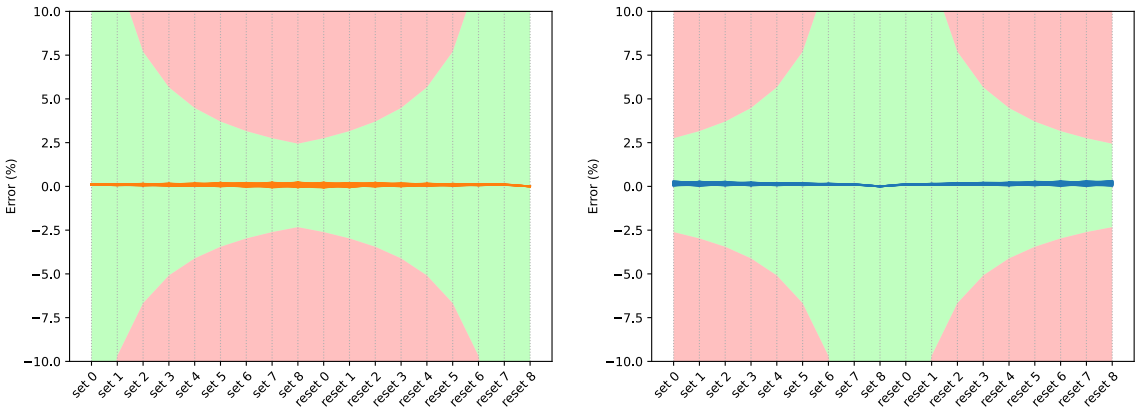


Fig. 11. Deviation from ideal resistance for the Normally Open (left) and Normally Closed (right) contacts.

TEST THREE – TEMPERATURE CYCLE TEST

In the third test, the temperature cycle test, the intention was to investigate how the relays performed during repeated temperature cycles between room temperature and cryogenic conditions. This would mimic the process of removing a test system from a cryostat for modification or room temperature evaluation before re-cooling the device. This is a common process within our labs. It was theorised that the repeated temperature cycles could cause the mechanical parts of the relays to expand and contract and potentially stick. It may also cause any volatile compounds released within the body of the relays at room temperature to condense on the coldest parts of the relay which, due to the relays being cooled via the test PCB, would be the contacts.

Procedure

The temperature cycle test consisted of alternating periods at room temperature (293 K) and cryogenic (60 K). The relays were held at 293 K for one hour, then ramped to 60 K at a rate of 2 K/min (over approximately two hours). They were then held at 60 K for one hour, before being ramped to 293 K at the same rate.

A delay of 240 s was inserted between each relay cycle to limit the number of operations performed at intermediate temperatures, and to reduce the amount of data generated over the long duration test.

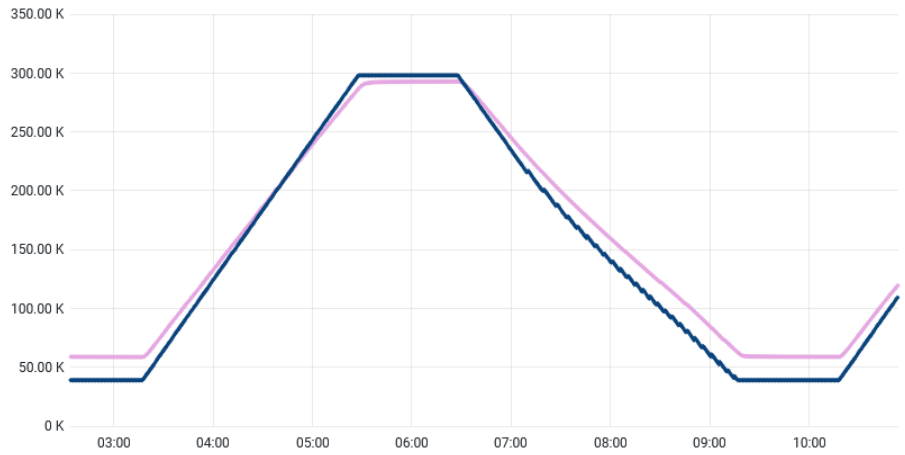


Fig. 12. An example temperature cycle. Blue is the cold plate temperature, and pink is the test PCB temperature.

Results

The test was run for 1,297 hours (54.0 days), for a total of 18,300 switching cycles (36,600 operations per relay) and 186 temperature cycles. Over the test period, a total of 409 failures were recorded, all but one of which was on Relay 1. Fig. 13 shows the log of relay failures over time for this test, and Fig. 14 shows the recorded values for deviation from the ideal resistance for each switching sequence.

At approximately 450 hours into the test, a single failure was recorded by the script against Relay 2. This was at the exact same time that Relay 1 started to exhibit significant non-compliant behaviour. Due to their adjacent switching in the test sequence, the authors believe that this failure was attributed to Relay 2 by mistake by the script but have chosen to include the unmodified results graphs.

The exact reason for the failures observed in Relay 1 are unclear – the failures occurred at different phases of the temperature cycles, and were not consistent with regard to which ‘direction’ of switching was affected (i.e. ‘Set’ to ‘Reset’ or vice versa). As nominal coil current was recorded during each failure and the NO and NC resiatances were unchanged (meaning that the closed contacts did not disengage), it can be seen that the issue was the relay entirely failing to togle state.

The only conclusion that can be reliably drawn from the information available is that the failures are occurring within the delicate mechanical components of the relay body. It should be noted that the removal of the caps, as described in the ‘Experimental Setup’ section, means that the relays are particularly sensitive to contamination.

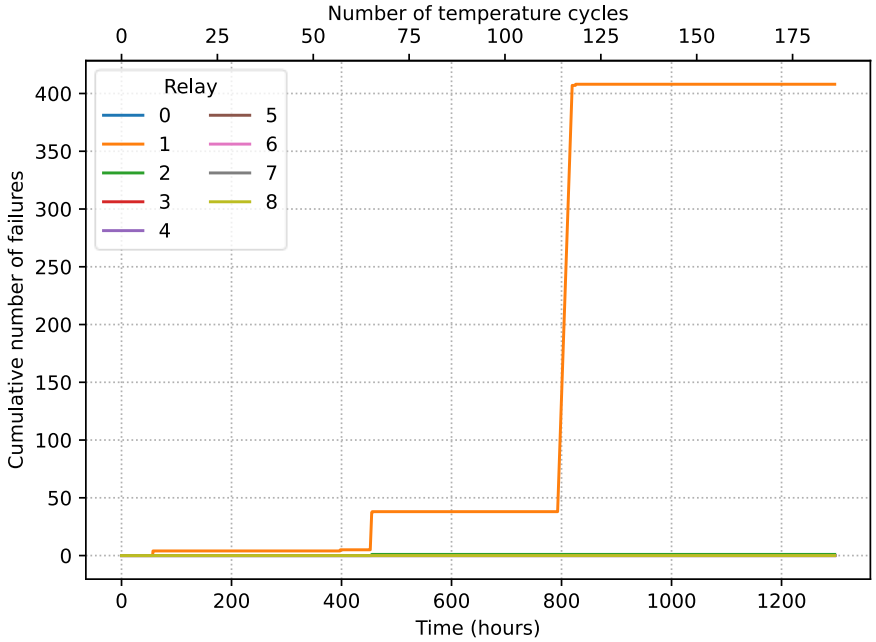


Fig. 13. Relay failures as a function of test time.

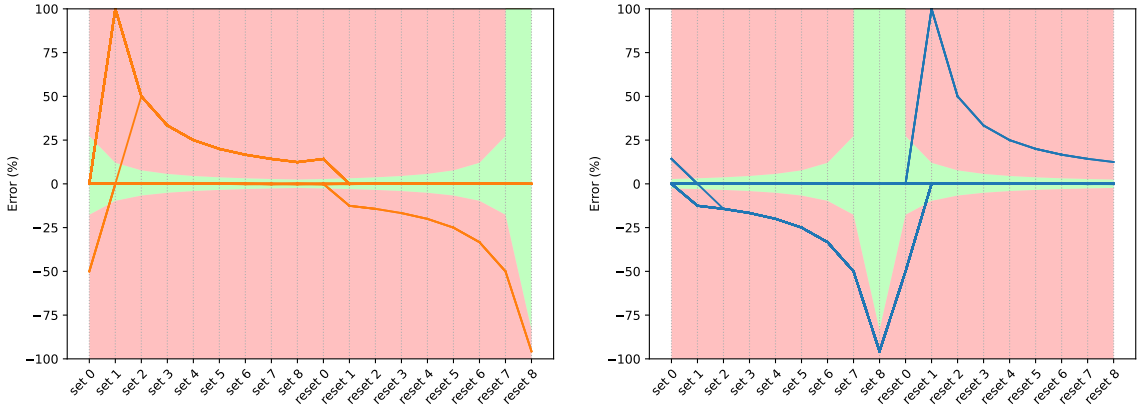


Fig. 14. Deviation from ideal resistance for the Normally Open (left) and Normally Closed (right) contacts.

TEST FOUR – MINIMUM TEMPERATURE TEST

In the fourth and final test, the minimum temperature test, the intention was to cool the relays further than would be required for normal operation in our lab and thus determine how close our operating temperatures are to the relay's limits. This test was performed last as it was expected to be destructive.

Procedure

In the minimum temperature test, the test script was started, and the relays then ramped to the lowest achievable temperature in the BOXY cryostat at a rate of 2 K/min. The script was then run for three days. Operating at the minimum temperature of the cryostat was achieved by setting a target temperature that was known to be impossible (10 K).
To get higher resolution view of the anticipated failure temperature, no delay was inserted between the relay cycles.

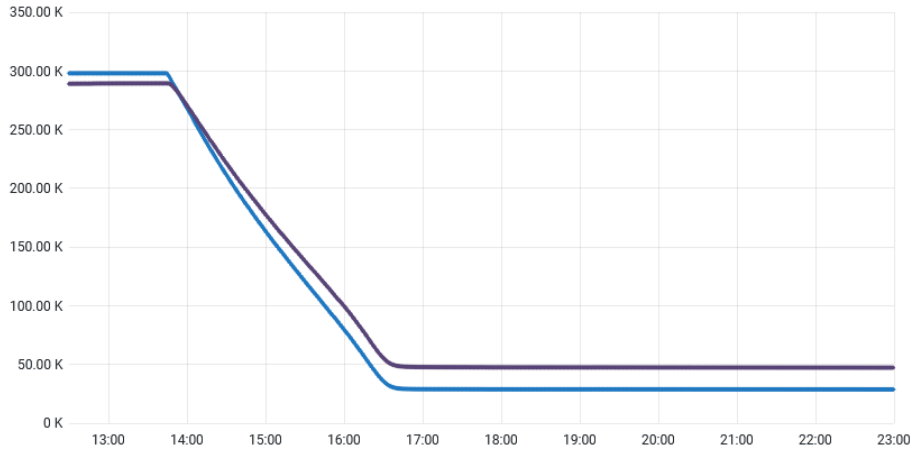


Fig. 15. Ramp to Min Temp. Blue is the cold plate temperature, and purple is the test PCB temperature.

Results

The test was run for 72 hours (3.0 days), for a total of 7,300 switching cycles (14,600 operations per relay). The minimum temperature achieved at the relay PCB was 47 K. This was likely constrained by the large thermal link produced by the thick cable harness.
Over the test period, no failures were observed on any of the nine relays. Fig. 16 shows the log of relay failures over time for this test, and Fig. 17 shows the recorded values for deviation from the ideal resistance for each switching sequence.

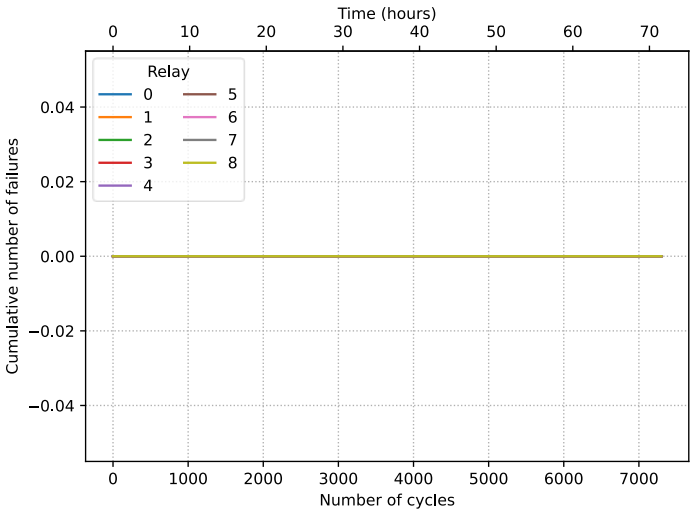


Fig. 16. Relay failures as a function of test time.

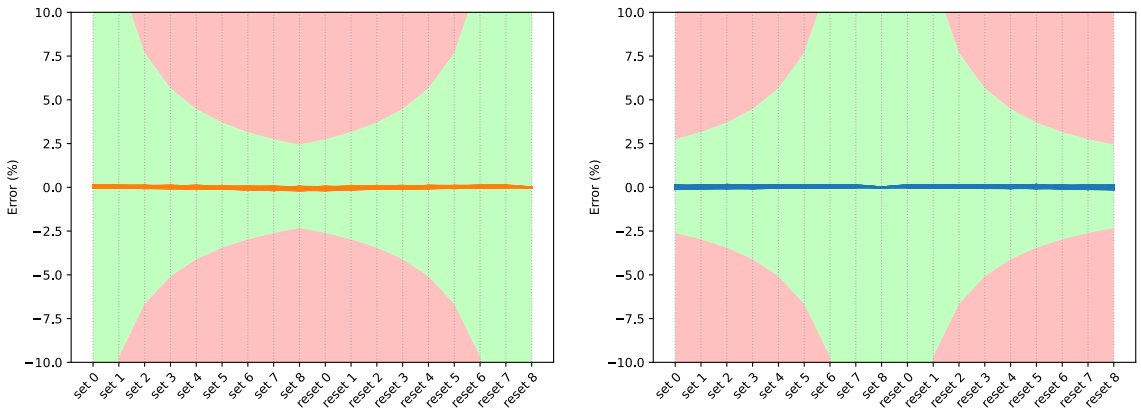


Fig. 17. Deviation from ideal resistance for the Normally Open (left) and Normally Closed (right) contacts.

LIMITATIONS OF TESTING

The testing performed during this evaluation process has some limitations which are worthy of note.

The testing described in this paper has placed the relays under no-load conditions only. This is due to our interest in the devices for small signal routing, rather than current carrying for power supplies. Use of the devices with more substantial currents across the contacts will reduce the lifespan considerably [2] and may also affect the reliability of the relays at cryogenic temperatures.

Despite the tests described here taking two months to complete, the relays reached only 0.59% of their rated no-load lifespan of 50,000,000 operations and have not been tested to destruction. The authors believe that the data presented demonstrates that the relays are suitable for lab use but could not justify the cryostat utilisation that would be required to test to 50,000,000 operations.

The small sample size of just nine relays should also be noted. Due to the relative ease of replacing a faulty component on a laboratory test PCB, the authors were willing to accept higher failure rates than would be demanded in industry or production environments. The testing here was intended to highlight any systematic issues with the devices under test that would preclude their use.

The same test PCB with the same nine relays was used for each test, and so the relays were not new at the start of each test. As each test completed, the subsequent test began with increasingly worn devices. This is of particular note in the temperature cycle test where failures were observed. Although failures were observed after less than 2,000 operations during the temperature cycle test, it must be noted that by this time the relays had already undergone over 245,000 operations in previous tests.

Due to the limitations of the cooling system on the cryostat used for this testing, the relays have not been tested down to extreme cryogenic temperatures. This is a notable point for applications in physics research systems, where to investigate atomic and quantum phenomena, temperatures in the single Kelvin range may be required.

Another potential limitation is the coil pulse duration used during testing. As noted in the test procedures, the coil pulse used for these tests was 500 ms, as opposed to the 10 ms minimum listed in the datasheet [2]. This was due to the cumulative script processing time, communication latency, and the switching speed of our Agilent 34970A Data Acquisition/Switch Unit. The behaviour of the relays at the minimum 10 ms coil pulse is therefore unknown.

CONCLUSIONS

The results of the four tests described here suggest that the Omron G6KU-2F-Y DC3 latching relay is suitable for use in the ESA lab environment where low current signals are switched at cryogenic temperatures.
The relay failures observed were only uncovered after dozens of temperature cycles and hundreds of thousands of relay operations, which is more than would normally be applied to a device under test in our labs. Additionally, as only one relay of the nine tested was affected by these failures, it appears that they may not be systemic or a result of the relay's design. More likely is that the failures on this individual relay were caused by contamination ingress into the device.

It is important to note briefly the behaviour of the relay coils at cryogenic temperatures. As discussed in the test procedures, both a voltage limit and a current limit were set on the power supplies. At room temperature, the supply was voltage limited (3 V), and at cryogenic temperatures the supply was in current limit (40 mA). This is a direct result of the relay coil being a standard ohmic conductor, whose resistivity decreases when cooled. This is important to note, as it demonstrates that current limiting must be factored into the design process for any drive electronics.

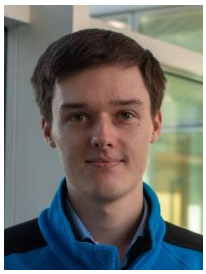
The authors finally wish to clearly state that despite the Omron G6KU-2F-Y DC3 latching relay being evaluated for use in space-like environments in the lab, that the data presented here does not represent space qualification.

REFERENCES

[1] J. E. Proctor, A. W. Smith, T. M. Jung and S. I. Woods, "High-gain cryogenic amplifier assembly employing a commercial CMOS operational amplifier," *Rev. Sci. Instrum.,* vol. 86, no. 7, July 2015.

[2] Omron, "G6K Surface Mounting Relay Datasheet," [Online]. Available: https://omronfs.omron.com/en_US/ecb/products/pdf/en-g6k.pdf. [Accessed 07 06 2024].

AUTHORS



Conor Robinson holds a Master of Engineering degree in Electrical and Electronic Engineering from the Queen's University of Belfast, Northern Ireland since 2016 and an Engineering Chartership from the Institution of Engineering and Technology in London since 2022. He is currently a Payload Technology Validation Engineer at the Science Directorate of the European Space Agency, working on the test and characterisation of payload technologies, as well as on the design of control and test electronics. He was previously employed by the UK's National Physical Laboratory, where he worked on the ESA LISA mission and on the design of compact atomic clocks.

Erik Ryman received the M.S. and PhD degree in electrical engineering from Chalmers University of Technology, Gothenburg, Sweden, in 2008 and 2018, respectively. He is currently working in the Science department's Payload Validation section at ESA/ESTEC with electronics for detector testing. He previously worked at Omnisys Instruments in Gothenburg, Sweden, on ASICs for signal processing and digitizing and power and control electronics for RF-instruments on missions such as ESA's Jupiter Icy Moons Explorer and Arctic Weather Satellite.

Sander Blommaert has a vast experience in manufacturing technology. He started at ESA/ESTEC Payload Validation Section as manufacturing specialist in 2007 and started designing test systems in 2015. He graduated for his engineering degree at Rotterdam university of applied sciences in January 2022 and is currently working section mechanics responsible. In the Payload validation section he worked on cryogenic test equipment for characterization of imaging sensors in support of ESA's science missions such as; CHEOPS, PLATO, ARIEL and EUCLID.

Evaluation of Automotive Grade Resistors for Space Flight

Zainab Abdullahi[(1)], Tristan Epp Schmidt[(1)], Susana Douglas[(1)], Timothy Mondy[(1)], Christopher Tiu[(1)]

[(1)] NASA Goddard Space Flight Center Code 562 Greenbelt, MD 20771 USA
Email: zainab.m.abdullahi@nasa.gov
Email:tristan.t.eppschmidt@nasa.gov
Email:susana.p.douglas@nasa.gov
Email:timothy.mondy@nasa.gov
Email:christopher.p.tiu@nasa.gov

ABSTRACT

Over the past decade, electronic, electrical, and electromechanical (EEE) parts for space applications have undergone significant changes, largely driven by CubeSat and commercial space developers pushing the boundaries on the utilization of commercial parts in space. Global product shortages and shipping delays are still impacting space flight project deadlines. Many projects have turned to automotive grade resistors as an alternate to their MIL-SPEC counterparts to fulfill requirements. In addition, automotive grade resistors may offer designers a wider range of parts to consider.

A recent NASA study recommended the use of high-volume manufactured commercial components for space applications provided these components show evidence of stringent fabrication controls and thorough reliability monitoring practices [1]. Automotive grade components have stringent qualification requirements, but the responsibility is on the user to assure parts compliance to datasheet specifications and to perform screening.

Screening, Life and Accelerated Life testing on a set of standard automotive-grade chip resistors is proposed to evaluate the reliability of these components. Requirements from both the AEC-Q (Automotive Electronic Council Qualification) and EEE-INST-002 (Instructions for EEE Parts Selection, Screening, Qualification, and Derating) for resistors is compared and discussed. The resistors have been tested by using a modified methodology from EEE-INST-002 to evaluate their reliability for space flight projects.

The findings of this study indicate that the underlying degradation mechanisms at rated temperature and power are best represented by power law models with a fitted exponent between 0 and 1. A linear model is more conservative which compensates for potential model uncertainty given the wide range of design and materials used in automotive resistors, while still providing useful long-term resistance drift estimates. No electrical anomalies or failures were observed throughout the 1000-hour Life Tests other than small in tolerance resistance drift aging. Degradation models were utilized to quantify and extrapolate the long-term resistance drift under operating conditions for the components. The models demonstrated that some automotive-grade resistors are likely to operate 10 years at nominal usage conditions while others might fail earlier.

INTRODUCTION

The methodology for using EEE components in NASA space applications is based on military standards established during the 1960's and 1970's [1]. The NASA EEE-INST-002 document was released in the early 2000's and establishes the baseline criteria for the selection, screening, qualification, and derating of EEE parts for use on NASA Goddard Space Flight Center (GSFC) space flight projects [2]. The AEC-Q200 document applies to passive components and outlines the minimum requirements for stress test driven qualification and details the test conditions required for qualifying these components [3]. The NASA Electronic Parts and Packaging (NEPP) Program has funded a study to assess the reliability of automotive grade chip resistors that have been qualified to the AEC-Q200

set of standards. A comparative study between the AEC-Q200 and EEE-INST-002 standards was conducted as shown in Figure 1 and a test plan for this study was developed consisting of a Screening, Life and an Accelerated Life Test.

NEPP Study Evaluation of Automotive Grade Resistors for Space	Test 1 Screening to EEE-INST-002, Table 2A	Test 2 Life Test (shall be from 100% screened samples)	Test 3 Accelerated Life Test (shall be from 100% screened samples)							
EEE-INST-002 Table 3A : Fixed Resistor Qualification Requirements	Group 1 Screening to Table 2A	Group 2 Solderability Resistance to Solvents	Group 3 Thermal Shock Resistance Temperature Characteristic Low Temperature Storage Low Temperature Operation Short-time Overload Terminal Strength Hermetic Seal	Group 4 Dielectric Withstanding Voltage Insulation Resistance Moisture Resistance Terminal Strength Hermetic Seal	Group 5 Shock Vibration, High Frequency Hermetic Seal	Group 6 Life	Group 7A Resistance to Bonding Moisture Resistance	Group 7B Adhesion	Group 8 Voltage Coefficient	Group 9 High Temperature Exposure	Group 10 Thermal Outgassing
AEC-Q200 (Rev E) Table 7B-5: Acceptance Criteria for SMD Chip Resistors	Test 1 Initial Limits (Pre- and Post Stress Electrical Test)	Test 3 High Temperature Exposure (storage)	Test 4 Temperature Cycling	Test 7 Biased Humidity	Test 8 Operational Life	Test 9 External Visual	Test 10 Physical Dimensions	Test 12 Resistance to Solvents	Test 13 Mechanical Shock	Test 14 Vibration	Test 15 Resistance to Soldering Heat
AEC-Q200 (Rev E) *continued* Table 7B-5: Acceptance Criteria for SMD Chip Resistors	Test 17 ESD	Test 18 Solderability	Test 19a Elec. Char. @25°C	Test 19b Elec. Char. @Min. operating temp	Test 19c Elec. Char. @Max operating temp.	Test 20 Flammability	Test 21 Board Flex (SMD)	Test 22 Terminal Strength (SMD)	Test 23 Flame Retardance		

Figure 1. Evaluation test flow used to assess reliability of Automotive Grade Chip Resistors

TEST DATA COLLECTION AND RESULTS

The Screening test flow was performed on all 9 resistor groups followed by the Life and Accelerated Life test flows performed on a sub-selection of the resistor groups that already completed Screening shown in Table 1.

Table 1. Summary of Resistor types evaluated and tests performed

Resistors Evaluated							Testing Performed		
Group ID (Part Number)	**Manufacturer**	**Resistance (Ω)**	**Tolerance (%)**	**Wattage (W)**	**Chip Size**	**Resistor Technology**	**Screening**	**Life**	**Accelerated Life**
A	A	0.1	0.5%	1	2512	Metal Strip	Yes	Yes	*No*
B	A	49.9	1%	0.25	1206	Thick Film	Yes	Yes	*No*
C	B	49.9	1%	0.1	0603	Thick Film	Yes	Yes	*No*
D	A	1,000	1%	0.25	1206	Thick Film	Yes	*No*	*No*
E	B	1,000	1%	0.1	0603	Thin Film	Yes	Yes	Yes
F	A	10,000	1%	0.25	1206	Thin Film	Yes	Yes	*No*
G	B	10,000	1%	0.1	0603	Thin Film	Yes	Yes	*No*
H	A	100,000	1%	0.25	1206	Thick Film	Yes	*No*	*No*
I	C	100,000	1%	0.1	0603	Thick Film	Yes	*No*	Yes

The Screening test consisted of both an initial and final external visual examination and Direct Current Resistance (DCR) measurements before and after thermal shock. The thermal shock test (per MIL-STD-202 Method 107) was performed utilizing the following conditions: [4]

- 100 cycles
- -55°C to +125°C
- 30-minute dwell time in air at temperature extremes

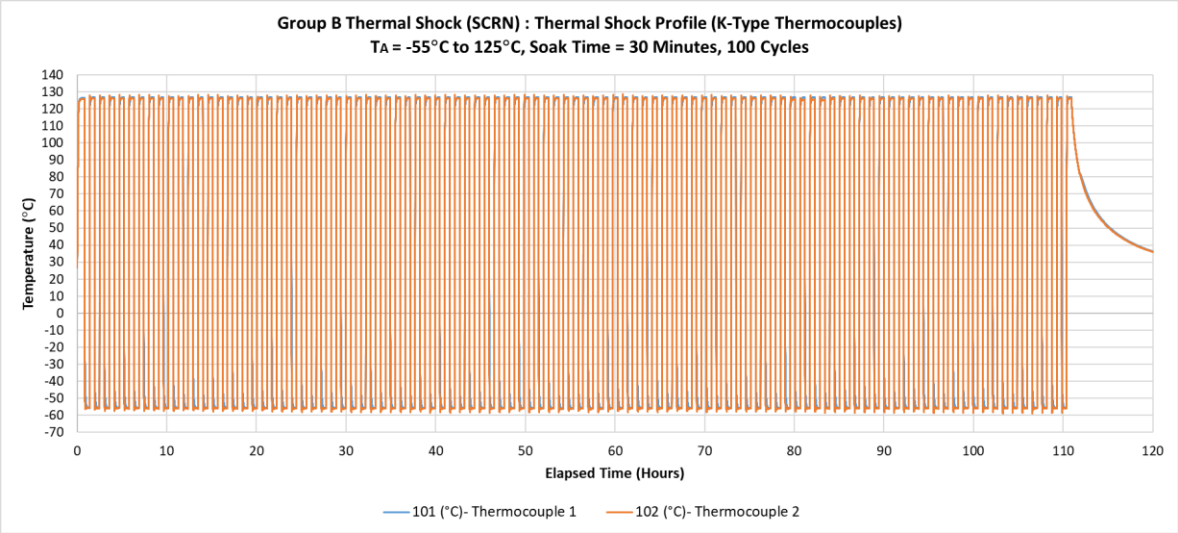


Figure 2. Thermal Shock temperature profile for Group B samples

DCR measurements (per MIL-STD-202, Method 303) were taken before and after thermal shock utilizing a Nano Volt Micro Ohm Meter [5]. A four-wire Kelvin measurement method was utilized so that the voltage drop in the test leads was eliminated and measured at the Device Under Test (DUT) shown in Figure 4.

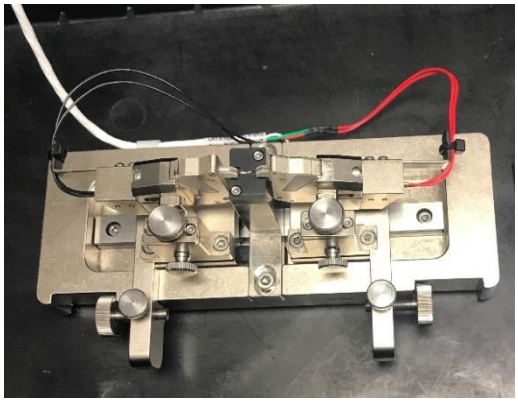


Figure 3. Test fixture used for obtaining DCR measurements

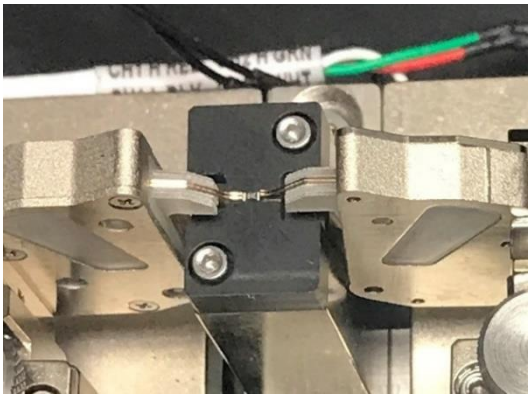


Figure 4. DUT in test fixture

The second test flow (Life Test) was performed on twenty samples from groups A, B, C, E, F and G. The twenty samples were mounted on Printed Circuit Boards (PCB) as shown in Figure 5. The samples were subjected to a 1,000-hour Life Test at 70°C and 1X rated power (90 minutes on, 30 minutes off). The samples were biased at the maximum working voltage $Vmax$ per the datasheet or the calculated voltage $Vrms$,whichever was less severe:

$$Vrms = \sqrt{PR}$$

where P is the maximum rated power and R is the nominal DC resistance value [6]. Various parameters were monitored during the 1,000-hour Life Test such as ambient temperature and the DCR measurements were obtained at 0, 100-, 250-, 500- and 1,000-hour increments.

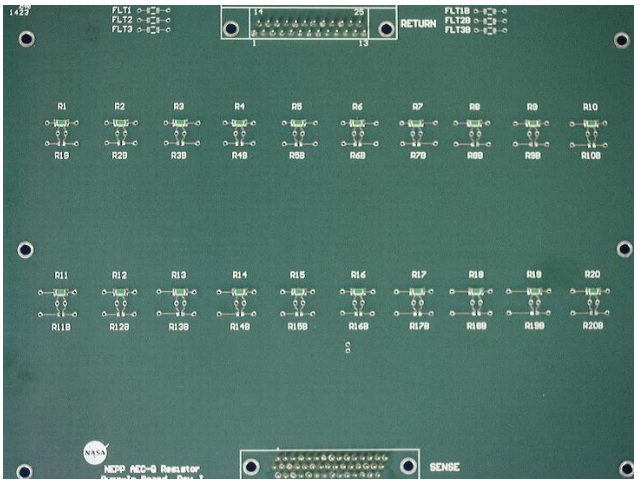


Figure 5. Life Test PCB used for Group F samples

The third test flow performed was an Accelerated Life Test. This test was performed on samples from Group E and Group I. This test flow consisted of various Life Test conditions including a test at 70°C at 0%, 70%, 120% and 150% applied power and an unbiased test at 155°C.

A single electrical failure was observed during the Screening Test (Group A, Serial Number 51) after the thermal shock test. This sample had an out of tolerance DCR per the datasheet specifications. All remaining samples passed DCR measurements per the datasheet specification limits.

DEGRADATION MODELS

Film resistors have generally been found to change in resistance as a function of time and temperature according to:

$$\frac{\Delta R}{R} = \sum_i a_i t^{b_i} \, exp\left(-\frac{E_A}{kT}\right)$$

where a_i and b_i relate to a particular aging mechanism. [7]

The resistance data at the 0-, 100-, 250-, 500-, and 1000-hour inspection points during the Life Test were pre-processed for analysis using the following:

$$R_{shift} = 100\% \cdot \frac{R_i - R_0}{R_0}$$

Where R_0 is the initial resistance and R_i are the resistances at each inspection interval. This results in the data being a percent shift from initial measurements.

The models considered were assessed for their predictive power using the Mean Square Error (MSE):

$$\text{MSE} = \frac{(y_i - \hat{y}_i)^2}{n}$$

where y_i is each measured percent resistance shift, $\hat{y}_i$ is the predicted percent resistance shift of the model and n is the number of data points. To assess the degradation model's ability to predict future resistance drifts, the measured data was separated into a training data set and a testing data set. The training data set was chosen to be the 0-, 100-, 250-, and 500-hour inspection data while the testing data was chosen to be the 1000-hour inspection data. The models were fit by regression on the testing data without having access to the 1000-hour inspection data. The

various resistance degradation models were assessed against their ability to predict the 1000-hour data using the MSE as shown in Table 2. The power law model performed the best across most of the groups (lowest testing data MSE). This confirms that resistance drift found in automotive grade resistors generally conform to the power law dependance degradation model.

Table 2: Various model performance predicting the 1000th hour resistance measurements when fit to the 0 to 500-hour resistance shift data

	$f(t) = \bar{y}$		$f(t) = mt + b$		$f(t) = mt$		$f(t) = at^b$	
Group ID	**MSE training**	**MSE Testing**	**MSE training**	**MSE Testing**	**MSE training**	**MSE Testing**	**MSE training**	**MSE Testing**
A	5.62E-05	1.97E-04	3.14E-05	5.45E-05	5.00E-05	3.05E-04	1.07E-05	3.70E-05
B	1.25E-06	2.35E-06	6.84E-07	3.66E-06	9.57E-07	8.48E-06	6.85E-06	1.22E-05
C	5.50E-05	1.47E-04	1.94E-05	1.71E-04	3.26E-05	4.59E-04	2.70E-06	9.73E-06
E	9.44E-06	5.01E-05	3.26E-06	1.34E-05	5.61E-06	2.27E-05	7.53E-06	7.86E-06
F	7.20E-08	3.13E-07	4.65E-08	1.30E-07	5.15E-08	2.34E-07	1.27E-07	8.93E-08
G	9.49E-07	1.10E-05	6.42E-07	1.45E-06	6.53E-07	1.32E-06	7.07E-07	4.50E-06
Total	2.02E-05	7.62E-05	9.16E-06	3.95E-05	1.48E-05	1.30E-04	4.79E-06	1.19E-05

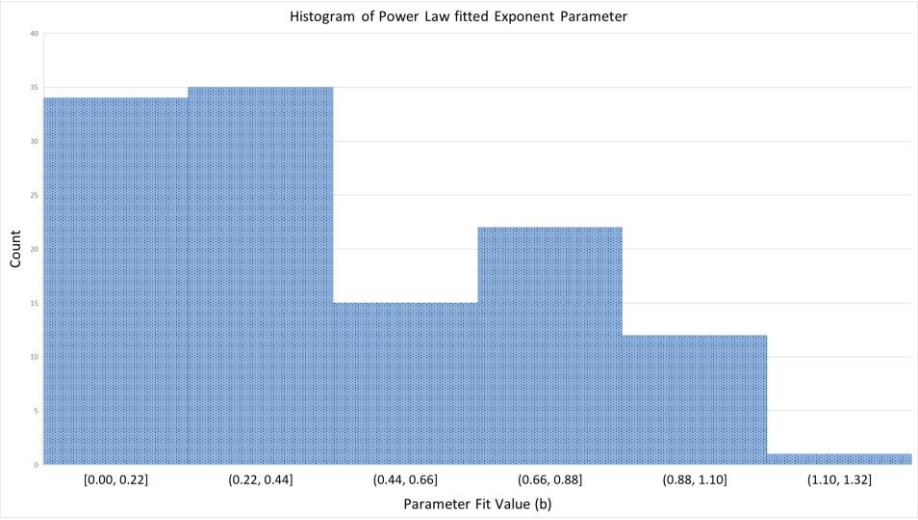


Figure 6: Histogram of the fitted power exponent for each of the 120 resistors that were life tested (Groups A, B, C, E, F, and G)

Out of 120 resistors that underwent Life Testing, only six (6) had a fit to the power law exponent greater than 1 with a maximum value of 1.12 (see Figure 6). All other 114 resistors had a fitted power law exponent less than 1. While the power law model may be better at prediction and a better fit to the data, the linear model in general is more conservative since the fitted power law exponent is less than 1 for almost all resistors in the dataset. This means that the linear model will grow more rapidly in general and reach earlier projected times to failure than the associated power law models.

MODEL PROJECTED FAILURE TIMES

Using a threshold for failure of a 1% resistance drift, we can project the degradation model forward in time until the threshold is met. These times are the projected times to failure for the resistor. Note that these are projected failure times and do not represent actual observed failures due to resistance drift. Reality in application may not conform to these laboratory test-based models. Using the linear resistance drift degradation model, we find the sudo-failure times shown in Figure 7 from our Life Test data.

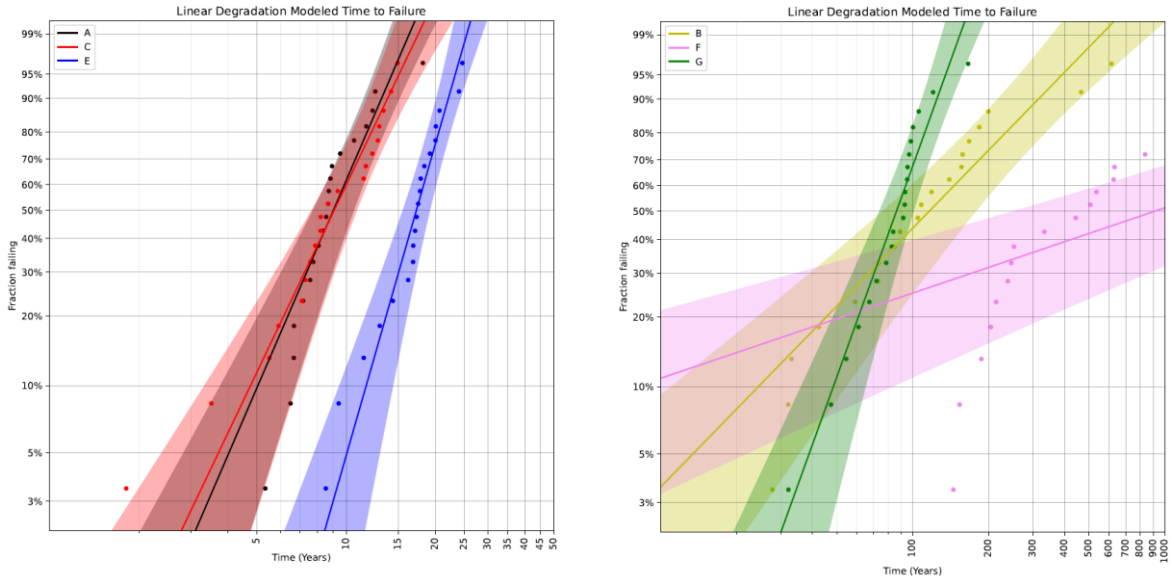


Figure 7: The projected times to failure shown on Weibull probability paper and found by extrapolating the Life Test data using the linear degradation model to a 1% resistance shift threshold. [8]

The parameters of the Weibull distribution fitted to the projected times to failure are given in Table 3.

Table 3: Weibull distribution fitted parameters to the projected times to failure using the linear degradation model.

	Alpha	**Beta**	**Earliest Projected Failure (yrs)**	**Projected TTF 50% (yrs)**
A	10.1	3.2	3.7	6
B	157	1.2	10	23
C	10.3	2.9	2.5	9
E	18.6	4.8	8	15
F	2296	0.4	97	203
G	96.4	3.2	14	80

SUMMARY AND CONCLUSIONS

Rigorous stress testing of 9 different automotive grade chip resistors demonstrated their durability under thermal shock, Life and Accelerated Life Test conditions. A single electrical failure was observed during the Screening Test (Group A, Serial Number 51) after the thermal shock test, with an out of tolerance DCR per the datasheet specifications. All remaining samples passed DCR measurements per the datasheet specification limits. However, the Life Test for this group revealed no failures. Life Test based models show that some automotive grade resistors are likely to last 10 years at nominal usage conditions while others might fail earlier. The extension of Life Tests is recommended to ensure that the proposed degradation models accurately reflect real long-term operating behavior.

ACKNOWLEDGEMENTS

The selection of parts for testing, formulation of test plans, execution of tests, and the subsequent data collection and analysis was performed at the NASA Goddard Space Flight Center (GSFC) Parts Analysis Laboratory, with support from EEE parts engineers in the GSFC Code 562 Parts, Packaging, and Assembly Branch. Significant contributors to this work include Jay Brusse, Lang Hua, Linh Le, Dr. Henning Leidecker, Lyudmyla Ochs, and Eugene Tayo. This study was funded by the NEPP Program, under the Mission Assurance Standards and Capabilities Division (MASCD) of the NASA Office of Safety and Mission Assurance (OSMA).

REFERENCES

[1] NASA Engineering and Safety Center. "*Recommendations on the Use of COTS EEE Parts for NASA Missions – Phase II."* NASA/TM−20220018183, 22 November 2022,

https://ntrs.nasa.gov/api/citations/20220018183/downloads/20220018183.pdf

[2] *Instructions for EEE Parts Selection, Screening, Qualification, and Derating*. EEE-INST-002. NASA/TP—2003–212242. NASA Goddard Space Flight Center. April 2008.

[3] *Stress Test Qualification for Passive Components.* AEC-Q200 Rev. E. Automotive Electronics Council. March 2023.

[4] *Department of Defense Test Method Standard, Method 107, Thermal Shock.* MIL-STD-202-107 Rev. H. Defense Logistics Agency. April 2015.

[5] *Department of Defense Test Method Standard, Method 303, DC Resistance*. MIL-STD-202-303 Rev. H. Defense Logistics Agency. April 2015.

[6] *General Specification for Resistor, Chip, Fixed, Film, Nonestablished Reliability, Established Reliability, Space Level.* MIL-PRF-55342 Rev. J. Defense Logistics Agency. May 2021.

[7] R. W. Kuehl, *"Stability of thin film resistors - Prediction and differences base on time-dependent Arrhenius law,"* Microelectronics Reliability 49, pp. 51-58, 2009.

[8] Reid, M. (2022). Reliability – a Python library for reliability engineering (Version 0.8.2) [Computer software]. Zenodo. https://doi.org/10.5281/ZENODO.3938000